Technical Note

Video Accessory IC Series

For portable image equipment Upscaler IC

BU1521GVW

No.09069EAT02

● Description

BU1521GVW upscales and interpolates images when upconverting to the HDTV (Maximum 1080P) format from the usual SDTV (NTSC/PAL) format.
High quality IP change・up scale management is realized by the frame memory less operate.
It is the LSI which is the most suitable for the compact system of the mobile.

● Features

1）Input format
480i or 576i(ITUR BT656) YCbCr 4:2:2(ITUR BT601) 8bit Digital Interface

2）Output Format
480i or 576i(ITUR BT656) YCbCr 4:2:2 8bit Digital Interface
480p or 576p(SMPTE 293・ITUR BT1358) YCbCr 4:2:2 16bit Digital Interface
1080/59.94i(SMPTE 274) YCbCr 4:2:2 16bit Digital Interface
1080/50i(SMPTE 274) YCbCr 4:2:2 16bit Digital Interface
1080/59.94p(SMPTE 274) YCbCr 4:2:2 16bit Digital Interface
1080/50p(SMPTE 274) YCbCr 4:2:2 16bit Digital Interface

3）IP conversion function
Conversion function from interlace to progressive

4）Upscale function
Horizontal direction: 720 pixels pass-through or upscaling to 1920 pixels
Vertical direction: up scaling to 480, 576, 540, and 1080 pixels

5）Filter function
5 × 5 filtering function over input data
Filter coefficient is programmable with registers

6）Register access
Register read/write through the SPI interface
Burst write/read support

7）Built-in PLL
Input frequency　27MHz
Output frequency　74.25MHz,74.175824MHz,148.5MHz,148.351648MHz

8）Power-down mode and through-mode support
Power-down mode can be controlled through STBY pin or register setting.
Through-mode can be selected by register setting.

9）Supply voltage
VDD(core voltage)1.15V～1.25V、AVDD(PLL)=2.7V~3.3V、
VDDIO1(SDTV input)=1.7V～3.6V、VDDIO2(control)=2.7V～3.3V、
VDDIO3(HDTV output)=1.7V～1.9V

10）Package
63 pin, BGA package (SBGA063W060, Size = 6 mm × 6 mm, 0.65 mm pitch)

● Aplications

Digital Video Camera、Digital still camera , Video game, a portable DVD

● Absolute Maximum Rating

Table. 1 Absolute maximum rating

Parameter	Symbol	Rating	Unit
Supply voltage 1 (SD input)	VDDIO1	-0.3～+4.2	V
Supply voltage 2 (Control)	VDDIO2	-0.3～+4.2	V
Supply voltage 3 (HD output)	VDDIO3	-0.3～+4.2	V
Supply voltage 4 (PLL)	AVDD	-0.3～+4.2	V
Supply voltage 5 (CORE)	VDD	-0.3～+1.68	V
Input voltage 1	VIN1	-0.3～VDDIO1+0.3	V
Input voltage 2	VIN2	-0.3～VDDIO2+0.3	V
Input voltage 3	VIN3	-0.3～VDDIO3+0.3	V
Storage temperature range	Tstg	-25～+125	ºC
Power dissipation	PD	330*1, 1200*2	mW

*1 IC only. In the case exceeding 25°C, 3.3 mW should be reduced at the rating 1°C.
*2 When packaging a glass epoxy board of 114.3 × 76.2 × 1.6 mm. In the case exceeding 25°C, 12 mW should be reduced at t he rating 1°C.
* Has not been designed to withstand radiation.
* Operation is not guaranteed.

● Operating Conditions

Table. 2 Operating conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage 1 (SD input)	VDDIO1	1.7	3.3	3.6	V
Supply voltage 2 (Control)	VDDIO2	2.7	3.0	3.3	V
Supply voltage 3 (HD output)	VDDIO3	1.7	1.8	1.9	V
Supply voltage 4 (PLL)	AVDD	2.7	3.0	3.3	V
Supply voltage 5 (CORE)	VDD	1.15	1.2	1.25	V
Operating temperature range	Topr	-25	-	85	℃

● Electrical Characteristics (DC Characteristics)

Table. 3 Electric characteristics

Parameter	Symbol	Specification			Unit	Conditions
		MIN	TYP	MAX		
Operational current (CORE)	IDD1	-	150	200	mA	When operated with HDCLK = 148.5 MHz
Operational current (IO)	IDD2	-	40	80	mA	When operated with HDCLK = 148.5 MHz and external capacitor of 5pF
Operational current (CORE)	IDD3	-	15	20	mA	When operated with DCLK = 27 MHz
Operational current (IO)	IDD4	-	10	20	mA	When operated with HDCLK = 27 MHz and external capacitor of 5pF
Static current	IDDst	-	-	800	μA	In standby mode
Input "H" current	IIH	-10	-	10	μA	VIH=VDDIO1/2
Input "L" current	IIL	-10	-	10	μA	VIL=GND
Input "H" voltage 1	VIH1	VDDIO1 *0.8	-	VDDIO1 +0.3	V	Ordinary input (Including input mode of I/O pin)
Input "L" voltage 1	VIL1	-0.3	-	VDDIO1 *0.2	V	Ordinary input (Including input mode of I/O pin)
Input "H" voltage 2	VIH2	VDDIO1 *0.85	-	VDDIO1 +0.3	V	Hysteresis input
Input "L" voltage 2	VIL2	-0.3	-	VDDIO1 *0.15	V	Hysteresis input
Hysteresis voltage range 2	Vhys2	-	0.75	-	V	Hysteresis input
Output "H" voltage 1	VOH1	VDDIO2 -0.4	-	VDDIO2	V	IOH1=-1.0mA(DC) SDOUT
Output "L" voltage 1	VOL1	0.0	-	0.4	V	IOL1=1.0mA(DC) SDOUT
Output "H" voltage 2	VOH2	VDDIO3 -0.2	-	VDDIO3	V	IOH1=-1.0mA(DC) HD output pin
Output "L" voltage 2	VOL2	0.0	-	0.2	V	IOL1=1.0mA(DC) HD output pin

(When not otherwise specified, under the conditions of VDD = 1.20 V, VDDIO1 = 3.3 V, VDDIO3 = 1.8 V, VDDIO2 = AVDD = 3.0 V, AVSS = GND = 0.0 V, and Ta = 25°C)

● Electrical Characteristics (AC Characteristics)

1. 3-wire serial interface timing

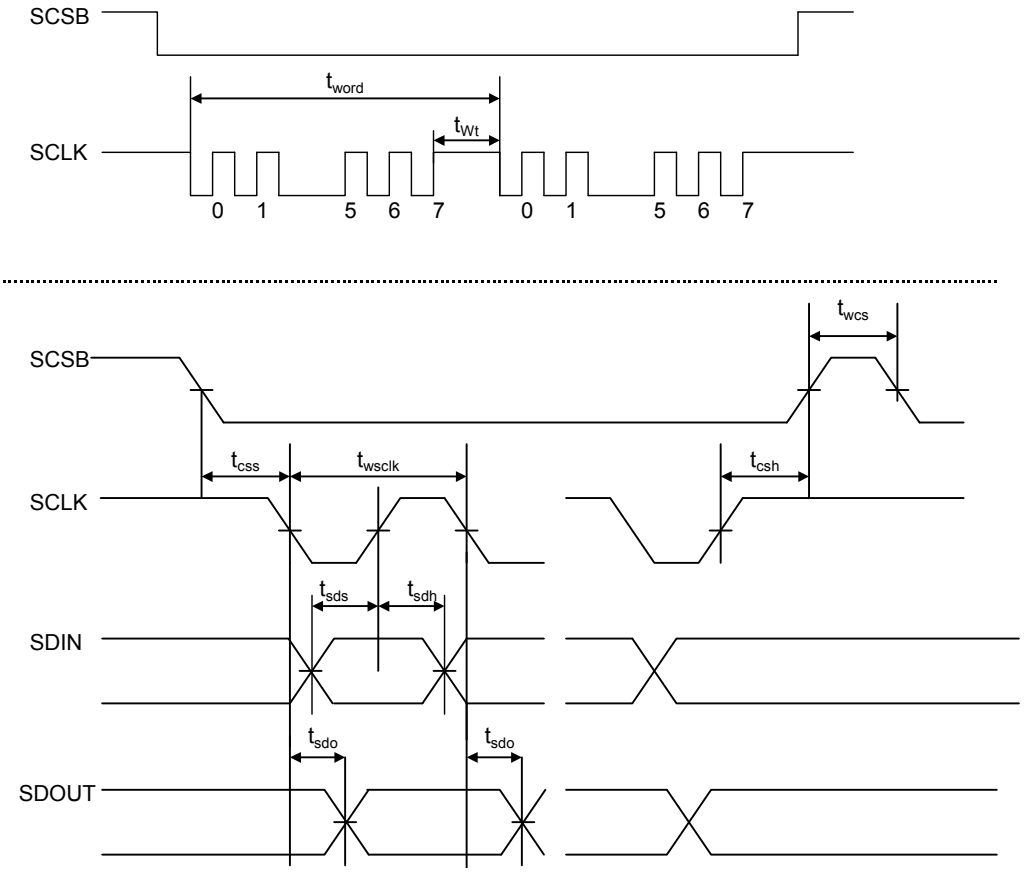


Fig. 1 3-wire serial interface format

Table. 4 3-wire serial interface format

Symbol	Description	MIN	TYP	MAX	Unit
t_{wsclk}	SCLK clock cycle	200	-	-	ns
t_{wcs}	SCSB access interval	1	-	-	μs
t_{css}	SCSB setup time	200	-	-	ns
t_{sds}	SDIN setup time	30	-	-	ns
t_{csh}	SCSB holding time	1	-	-	μs
t_{sdh}	SDIN holding time	30	-	-	ns
t_{sdo}	Time from trailing of the clock to the establishment of SDOUT	-	-	60	ns
t_{word}	1 word write time	2.5	-	-	μs
t_{wt}	1 word write interval	1	-	-	μs

2. Image Data Input Timing

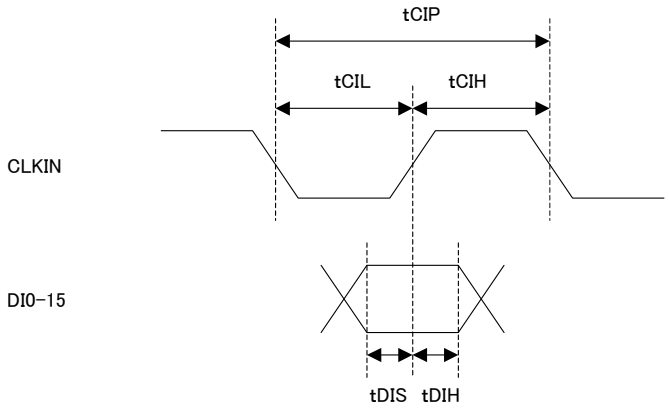


Fig. 2 Image Data Input Timing

Table. 5 Image Data Input Timing

Symbol	Description	MIN	TYP	MAX	Unit
t_{CIP}	CLKIN Clock cycle	-	37.03	-	ns
d_{CKI}	CLKIN clock duty (tCIL/tCIP or tCIH/tCIP)	45	50	55	%
t_{DIS}	Data setup time from the CLKIN rise	2	-	-	ns
t_{DIH}	Data holding time from the CLKIN rise	3	-	-	ns

3. Image Data Output Timing

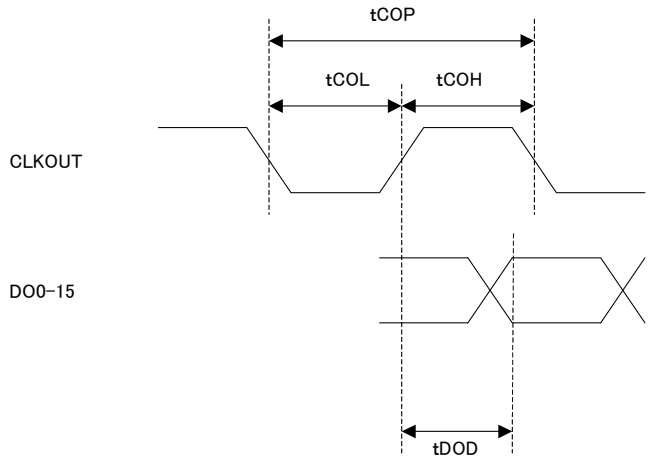


Fig. 3 Image Data Output Timing

Table. 6 Image Data Output Timing

Symbol	Description	MIN	TYP	MAX	Unit
t_{COP}	CLKOUT Clock cycle	6.734	-	-	ns
d_{CKO}	CLKOUT clock duty (tCOL/tCOP or tCOH/tCOP) *	45	-	55	%
t_{DOD}	Time from the rise of CLKOUT to the establishment of DO0-15	1	-	12	ns
t_{DOD}	Time from the rise of CLKOUT to the establishment of DO0-15	1	-	5.734	ns
t_{JIT}	Output jitter of CLKOUT (1 us cycle)	-	-	2	ns

* When PLL is used. When 27 MHz is output, the input clock duty is 50%.

- Pin configuration diagram (Bottom View)

Fig. 4 Pin configuration diagram of BU1521GVW (Bottom view).

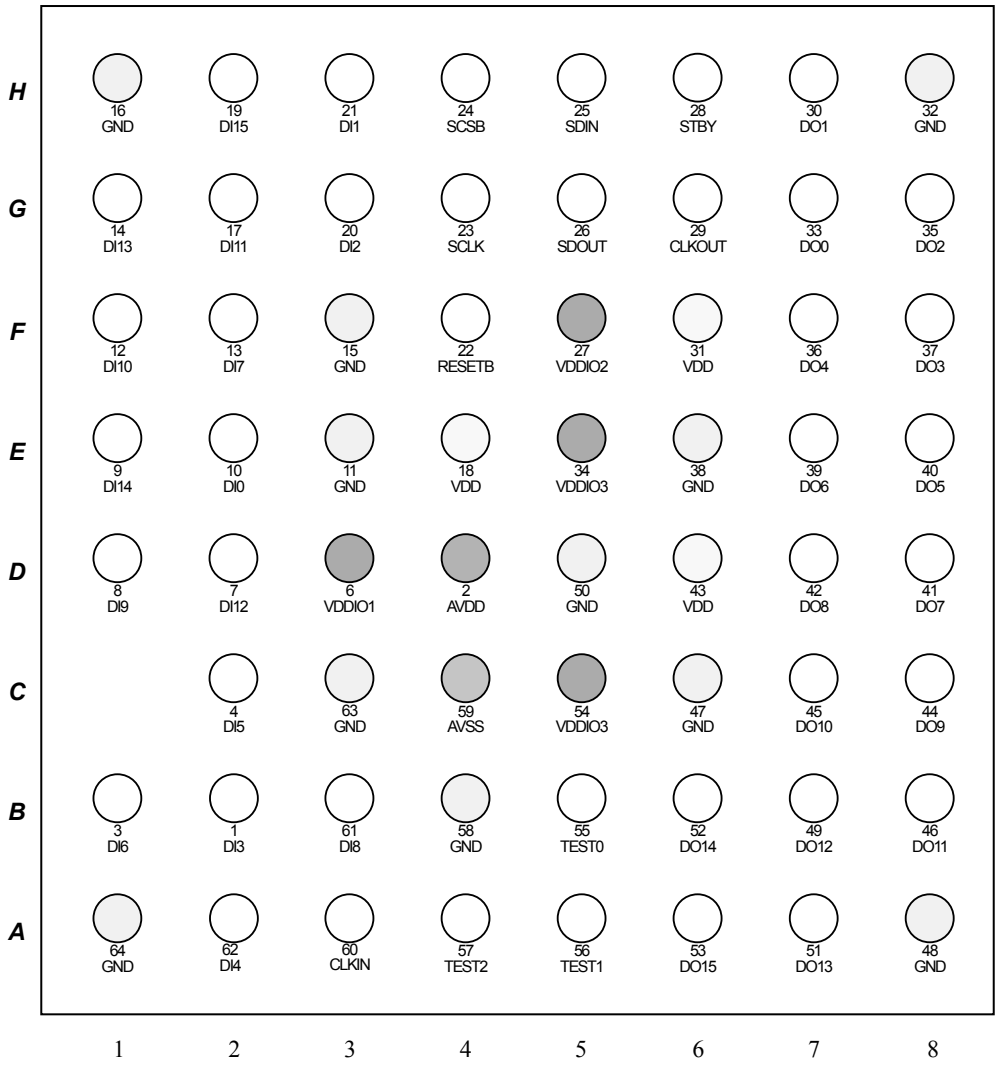


Fig. 4 BU1521GVW Pin configuration diagram(Bottom View)

● Pin Function

Table. 7 BU1521GVW terminal function(1)

PIN No.	Ball No.	PIN Name	In/Out	Init	Function Description	I/O Type	I/O System
1	B2	DI3	In	–	3rd bit of SD input data	B	VDDIO1
2	D4	AVDD	–	–	Power Source for PLL	–	–
3	B1	DI6	In	–	6th bit of SD input data	B	VDDIO1
4	C2	DI5	In	–	5th bit of SD input data	B	VDDIO1
5	–	N.C *1	–	–	–	–	–
6	D3	VDDIO1	–	–	Data input IO voltage (Typical 3.3 V)	–	–
7	D2	DI12	In	–	12th bit of SD input data	B	VDDIO1
8	D1	DI9	In	–	9th bit of SD input data	B	VDDIO1
9	E1	DI14	In	–	14th bit of SD input data	B	VDDIO1
10	E2	DI0	In	–	0th bit of SD input data	B	VDDIO1
11	E3	GND	–	–	GND	–	–
12	F1	DI10	In	–	10th bit of SD input data	B	VDDIO1
13	F2	DI7	In	–	7th bit of SD input data	B	VDDIO1
14	G1	DI13	In	–	13th bit of SD input data	B	VDDIO1
15	F3	GND	–	–	GND	–	–
16	H1	GND	–	–	GND	–	–
17	G2	DI11	In	–	11th bit of SD input data	B	VDDIO1
18	E4	VDD	–	–	Core power supply (1.2 V)	–	–
19	H2	DI15	In	–	15th bit of SD input data	B	VDDIO1
20	G3	DI2	In	–	2nd bit of SD input data	B	VDDIO1
21	H3	DI1	In	–	1st bit of SD input data	B	VDDIO1
22	F4	RESETB	In	–	Reset pin (low active)	B*2	VDDIO2
23	G4	SCLK	In	–	3-wire serial I/F clock	B*2	VDDIO2
24	H4	SCSB	In	–	3-wire serial I/F chip select	B*2	VDDIO2
25	H5	SDIN	In	–	3-wire serial I/F data input	B*2	VDDIO2
26	G5	SDOUT	Out	Low	3-wire serial I/F data output	C*3	VDDIO2
27	F5	VDDIO2	–	–	Control signal IO voltage (typically 3.3 V)	–	–
28	H6	STBY	In	–	IC stand-by control	A	VDDIO2
29	G6	CLKOUT	Out	Low	HD clock output	D	VDDIO3
30	H7	DO1	Out	PD	1st bit of HD output pin	C	VDDIO3
31	F6	VDD	–	–	Core power supply (1.2 V)	–	–
32	H8	GND	–	–	GND	–	–
33	G7	DO0	Out	PD	0th bit of HD output pin	C	VDDIO3
34	E5	VDDIO3	–	–	Data output IO voltage (typically 1.8 V)	–	–
35	G8	DO2	Out	PD	2nd bit of HD output pin	C	VDDIO3
36	F7	DO4	Out	PD	4th bit of HD output pin	C	VDDIO3
37	F8	DO3	Out	PD	3rd bit of HD output pin	C	VDDIO3
38	E6	GND	–	–	GND	–	–
39	E7	DO6	Out	PD	6th bit of HD output pin	C	VDDIO3
40	E8	DO5	Out	PD	5th bit of HD output pin	C	VDDIO3
41	D8	DO7	Out	PD	7th bit of HD output pin	C	VDDIO3

Table. 8 BU1521GVW terminal function(2)

PIN No.	Ball No.	PIN Name	In/Out	Init	Function Description	I/O Type	I/O System
42	D7	DO8	Out	PD	8th bit of HD output pin	C	VDDIO3
43	D6	VDD	–	–	Core power supply (1.2 V)	–	–
44	C8	DO9	Out	PD	9th bit of HD output pin	C	VDDIO3
45	C7	DO10	Out	PD	10th bit of HD output pin	C	VDDIO3
46	B8	DO11	Out	PD	11th bit of HD output pin	C	VDDIO3
47	C6	GND	–	–	GND	–	–
48	A8	GND	–	–	GND	–	–
49	B7	DO12	Out	PD	12th bit of HD output pin	C	VDDIO3
50	D5	GND	–	–	GND	–	–
51	A7	DO13	Out	PD	13th bit of HD output pin	C	VDDIO3
52	B6	DO14	Out	PD	14th bit of HD output pin	C	VDDIO3
53	A6	DO15	Out	PD	15th bit of HD output pin	C	VDDIO3
54	C5	VDDIO3	–	–	Data output IO voltage (Typical 1.8 V)	–	–
55	B5	TEST0	In	–	Test pin 0 (Connect to GND)	A	VDDIO3
56	A5	TEST1	In	–	Test pin 1 (Connect to GND)	A	VDDIO3
57	A4	TEST2	In	–	Test pin 2 (Connect to GND)	A	VDDIO3
58	B4	GND	–	–	GND	–	–
59	C4	AVSS	–	–	GND for PLL	–	–
60	A3	CLKIN	In	–	SD clock input (27 MHz)	B	VDDIO1
61	B3	DI8	In	–	8th bit of SD input data	B	VDDIO1
62	A2	DI4	In	–	4th bit of SD input data	B	VDDIO1
63	C3	GND	–	–	GND	–	–
64	A1	GND	–	–	GND	–	–

Init column indicates pin status when released from reset. Low: L output PD: Pull-down

*1: No balls *2: Input suspend function is fixed to OFF by an internal signal *3: No pull-down function

● Block Diagram

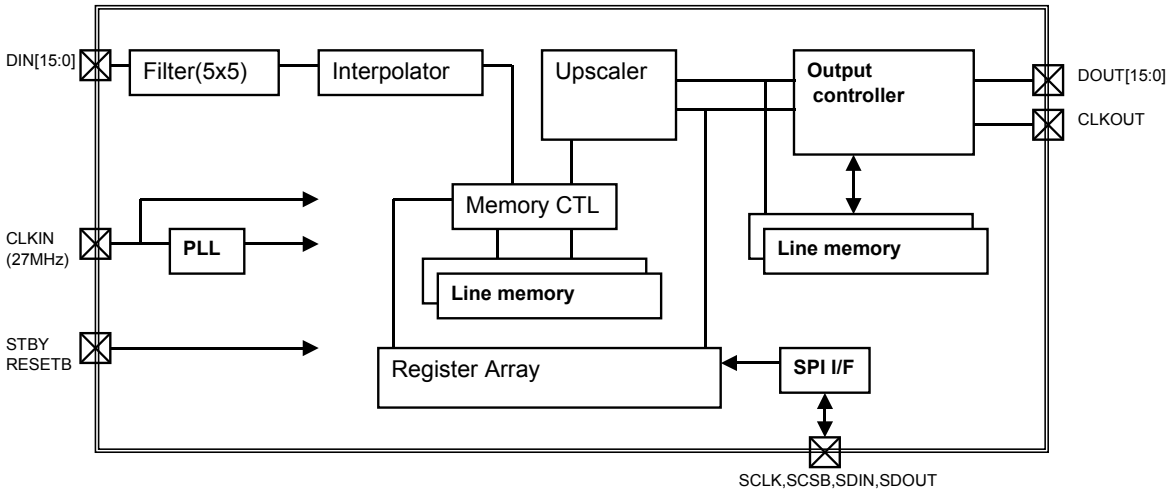


Fig. 5 BU1521GVW Block diagram

● Functions Discpriction

1. Input format

The following is the input format for BU1521GVW

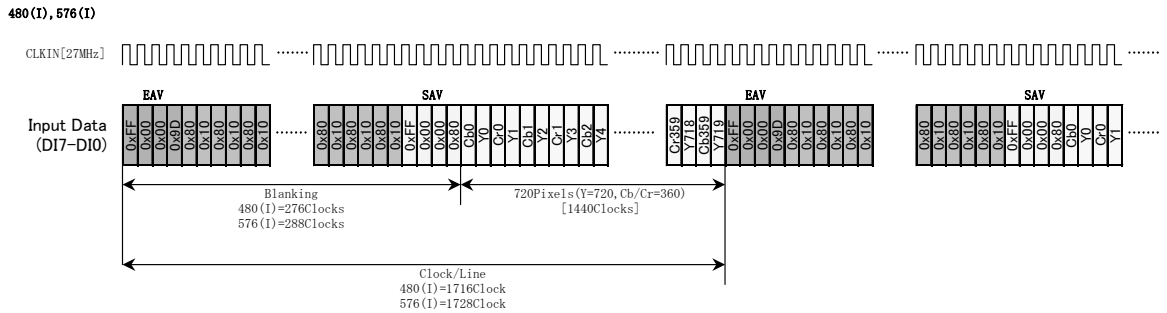
480i or 576i(ITUR BT656) YCbCr 4:2:2 8bit(ITUR BT601) Digital Interface

Table. 9 Input format

Format	Data bit width	Pixel clock (MHz)	Size including blank (HxV)	Active Size (HxV)	Standard
480/59.94i	8	27	858x525	720x(244/243)	ITUR BT656-4
576/50i	8	27	864x625	720x(288/288)	

SYS2 register (0 × 12) setting allows applying whether Y data and CbCr data to be assigned to lower DI [7:0] or upper DI [15:8].

2. Output format



The following is the output format for BU1521GVW:

480i or 576i(ITUR BT656) YCbCr 4:2:2 8bit (ITUR BT601)Digital Interface
480p or 576p(ITUR BT1358) YCbCr 4:2:2 16bit(ITUR BT601) Digital Interface
1080/59.94i(SMPTE 274) YCbCr 4:2:2 16bit(ITUR BT601) Digital Interface
1080/50i(SMPTE 274) YCbCr 4:2:2 16bit(ITUR BT601) Digital Interface
1080/59.94p(SMPTE 274) YCbCr 4:2:2 16bit(ITUR BT601) Digital Interface
1080/50p(SMPTE 274) YCbCr 4:2:2 16bit(ITUR BT601) Digital Interface

Table. 10 Output format

Format	Data bit width	Pixel Clock Frequency (MHz)	Blanking Size including Line (HxV)	Active Image Size (HxV)	Standard
480/59.94i	8	27	858x525	720x(244/243)	ITUR BT656-4
576/50i	8	27	864x625	720x(288/288)	
480/59.94p	16	27	858x525	720x483	ITUR BT1358 SMPTE 293M
576/50p	16	27	864x625	720x576	
1080/59.94i	16	74.25/1.001	2200x1125	1920x1080	SMPTE 274
1080/50i	16	74.25	2640x1125	1920x1080	
1080/59.94p	16	148.5/1.001	2200x1125	1920x1080	
1080/50p	16	148.5	2640x1125	1920x1080	

3. IP conversion, upscale function

BU1521GVW upscales and interpolates images when upconverting to output format.

Supported image data I/O conversion is shown in Table. 11 .

Only input size of 720 or upscale to 1920 are supported for the horizontal direction.

The edge of the upscaled image can be enhanced (3 levels) by changing the UPC_SEL register.

When upscaling the 480i input, upscaling is applied to 240 lines among the overall effective lines

Table. 11 Image data I/O conversion table

Input (SD)	Output (HD)							
	480/ 59.94i	480/ 59.94p	576/ 50i	576/ 50p	1080/ 59.94i	1080/ 50i	1080/ 59.94p	1080/ 50p
480/59.94i	○	○※	–	–	○	–	○	–
576/50i	–	–	○	○	–	○	–	○

* Immediately after reset and when standby mode is set, 480i becomes 480p.

4. Filter fiunction

BU1521GVW can apply 5 taps of filtering both horizontally and vertically.

5 taps of filter tap coefficients can be set independently on horizontal and vertical directions using filter coefficient registers (0x14–0x1B).

5 x 5 Filter tap coefficients = Horizontal filter tap coefficients x Vertical filter tap coefficients.

The values of the horizontal and vertical filter taps must be set to make the sum of the coefficients 64.

The initial value makes the filter invalid.

[Horizontal filter tap coefficients]

1	2	3	4	5	
TH1	TH2	TH3	TH4	TH5	/64

[Vertical filter tap coefficients]

1	TV1	
2	TV2	
3	TV3	
4	TV4	
5	TV5	/64

[5 × 5 filter tap coefficients]

行番号	列番号					
	1	2	3	4	5	
1	TH1*TV1	TH2*TV1	TH3*TV1	TH4*TV1	TH5*TV1	
2	TH1*TV2	TH2*TV2	TH3*TV2	TH4*TV2	TH5*TV2	
3	TH1*TV3	TH2*TV3	TH3*TV3	TH4*TV3	TH5*TV3	
4	TH1*TV4	TH2*TV4	TH3*TV4	TH4*TV4	TH5*TV4	
5	TH1*TV5	TH2*TV5	TH3*TV5	TH4*TV5	TH5*TV5	/4096

Fig. 6 5 × 5 filter tap coefficients

5. Register access

Registers are accessed by 3 wire serial interfaces (SCSB, SCLK, SDIN, SDOUT).
Burst write/read is supported; therefore, consecutive writing is possible.

◆ Regular write sequence

The address 8 bits and data 8 bits should be written in this order.
Both address and data have MSB first.

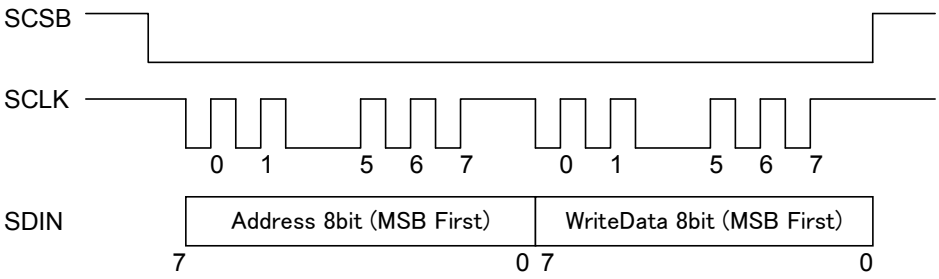


Fig. 7 Regular write sequence

◆ Regular read sequence

For reading, the address of the register to be read out should be written in the SADR register (0 × 70), then SRDAT register (0 × 80) should be read out. Both address and data have MSB first.

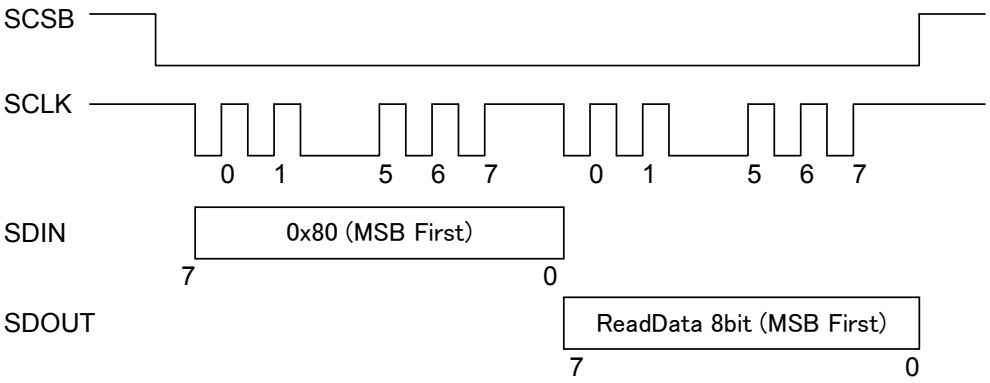


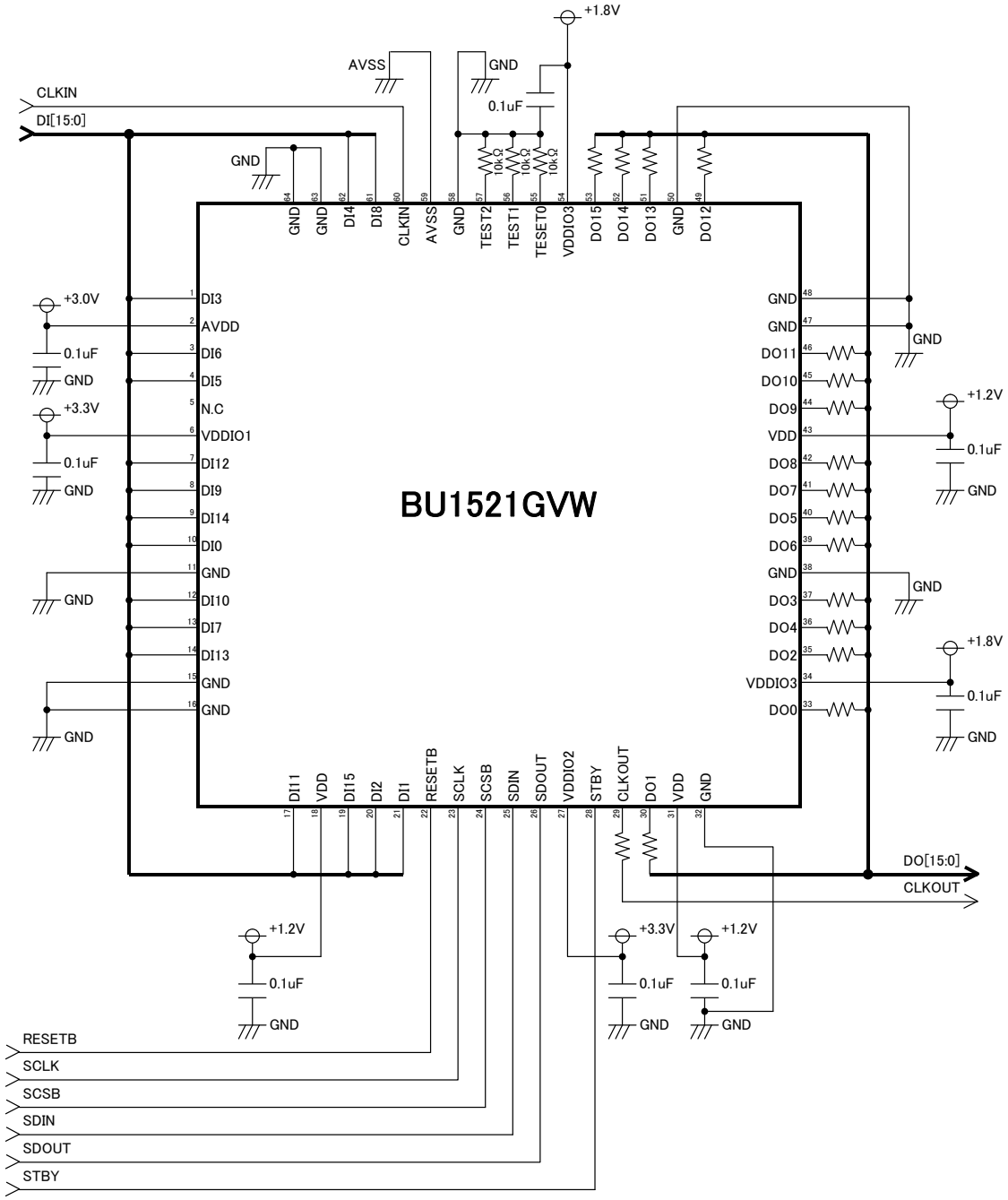
Fig. 8 Regular read sequence

6. PLL

BU1521GVW has an integrated PLL to generate and output the clock for HD format from the 27 MHz pixel clock.
The PLL output frequency is selected and output is executed according to the output format only, by setting the output format to the register.
The input frequency is 27 MHz and the output frequency can be 74.25 MHz, 74.25/1.001 MHz, 148.5 MHz, or 148.5/1.001 MHz.
With 480i/576i output format, the 27 MHz input clock is output without going through the PLL.

● Typical application circuit

The typical application circuit of BU1521GVW is shown in Fig. 9 It does not guarantee



Note 1) Adjust the output damping resistance for CLKOUT and DO [15:0] with the line load.

Note 2) When the STBY pin is unused, pull it down with a 10 kΩ resistor.

Fig. 9 BU1521GVW typical application circuit

● I/O pin equivalent circuit diagram

Fig. 10 An I/O pin equivalent circuit diagram.

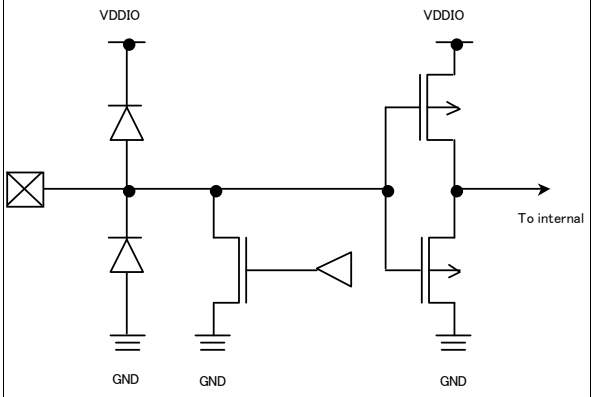
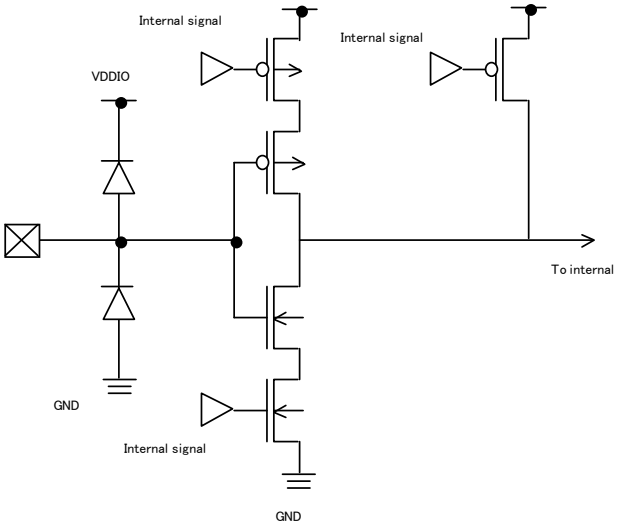
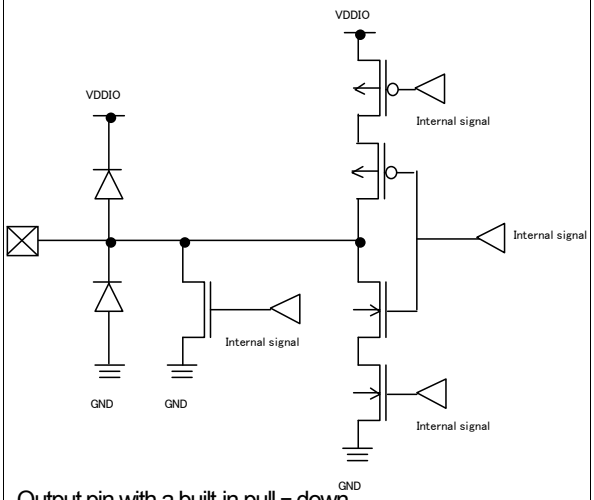
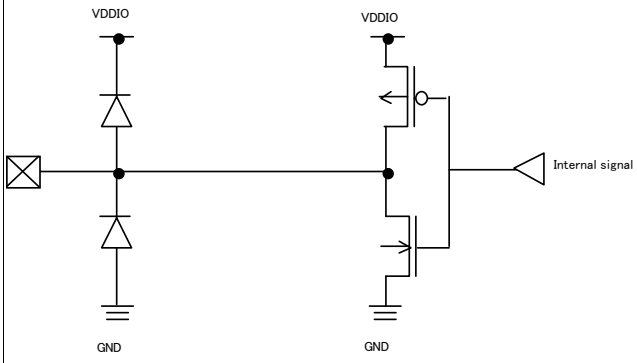
Type	The equivalent circuit structure	Type	The equivalent circuit structure
A	 Input pin with Pull－Down	B	 Input pin with hysteresis and suspend
C	 Output pin with a built-in pull－down	D	 Output pin

Fig. 10　BU1521GVW I/O pin equivalent circuit diagram

● Not for uses

(1) Absolute Maximum Ratings

An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down devices, thus making impossible to identify breaking mode such as a short circuit or an open circuit. If any special mode exceeding the absolute maximum ratings is assumed, consideration should be given to take physical safety measures including the use of fuses, etc.

(2) Operating conditions

These conditions represent a range within which characteristics can be provided approximately as expected. The electrical characteristics are guaranteed under the conditions of each parameter.

(3) Reverse connection of power supply connector

The reverse connection of power supply connector can break down ICs. Take protective measures against the breakdown due to the reverse connection, such as mounting an external diode between the power supply and the IC's power supply terminal.

(4) Power supply line

Design PCB pattern to provide low impedance for the wiring between the power supply and the GND lines.

In this regard, for the digital block power supply and the analog block power supply, even though these power supplies has the same level of potential, separate the power supply pattern for the digital block from that for the analog block, thus suppressing the diffraction of digital noises to the analog block power supply resulting from impedance common to the wiring patterns. For the GND line, give consideration to design the patterns in a similar manner.

Furthermore, for all power supply terminals to ICs, mount a capacitor between the power supply and the GND terminal. At the same time, in order to use an electrolytic capacitor, thoroughly check to be sure the characteristics of the capacitor to be used present no problem including the occurrence of capacity dropout at a low temperature, thus determining the constant.

(5) GND voltage

Make setting of the potential of the GND terminal so that it will be maintained at the minimum in any operating state. Furthermore, check to be sure no terminals are at a potential lower than the GND voltage including an actual electric transient.

(6) Short circuit between terminals and erroneous mounting

In order to mount ICs on a set PCB, pay thorough attention to the direction and offset of the ICs. Erroneous mounting can break down the ICs. Furthermore, if a short circuit occurs due to foreign matters entering between terminals or between the terminal and the power supply or the GND terminal, the ICs can break down.

(7) Operation in strong electromagnetic field

Be noted that using ICs in the strong electromagnetic field can malfunction them.

(8) Inspection with set PCB

On the inspection with the set PCB, if a capacitor is connected to a low-impedance IC terminal, the IC can suffer stress. Therefore, be sure to discharge from the set PCB by each process. Furthermore, in order to mount or dismount the set PCB to/from the jig for the inspection process, be sure to turn OFF the power supply and then mount the set PCB to the jig. After the completion of the inspection, be sure to turn OFF the power supply and then dismount it from the jig. In addition, for protection against static electricity, establish a ground for the assembly process and pay thorough attention to the transportation and the storage of the set PCB.

(9) Input terminals

In terms of the construction of IC, parasitic elements are inevitably formed in relation to potential. The operation of the parasitic element can cause interference with circuit operation, thus resulting in a malfunction and then breakdown of the input terminal. Therefore, pay thorough attention not to handle the input terminals, such as to apply to the input terminals a voltage lower than the GND respectively, so that any parasitic element will operate. Furthermore, do not apply a voltage to the input terminals when no power supply voltage is applied to the IC. In addition, even if the power supply voltage is applied, apply to the input terminals a voltage lower than the power supply voltage or within the guaranteed value of electrical characteristics.

(10) Ground wiring pattern

If small-signal GND and large-current GND are provided, It will be recommended to separate the large-current GND pattern from the small-signal GND pattern and establish a single ground at the reference point of the set PCB so that resistance to the wiring pattern and voltage fluctuations due to a large current will cause no fluctuations in voltages of the small-signal GND. Pay attention not to cause fluctuations in the GND wiring pattern of external parts as well.

(11) External capacitor

In order to use a ceramic capacitor as the external capacitor, determine the constant with consideration given to a degradation in the nominal capacitance due to DC bias and changes in the capacitance due to temperature, etc.

● External Dimensional Drawing and Mark Drawing

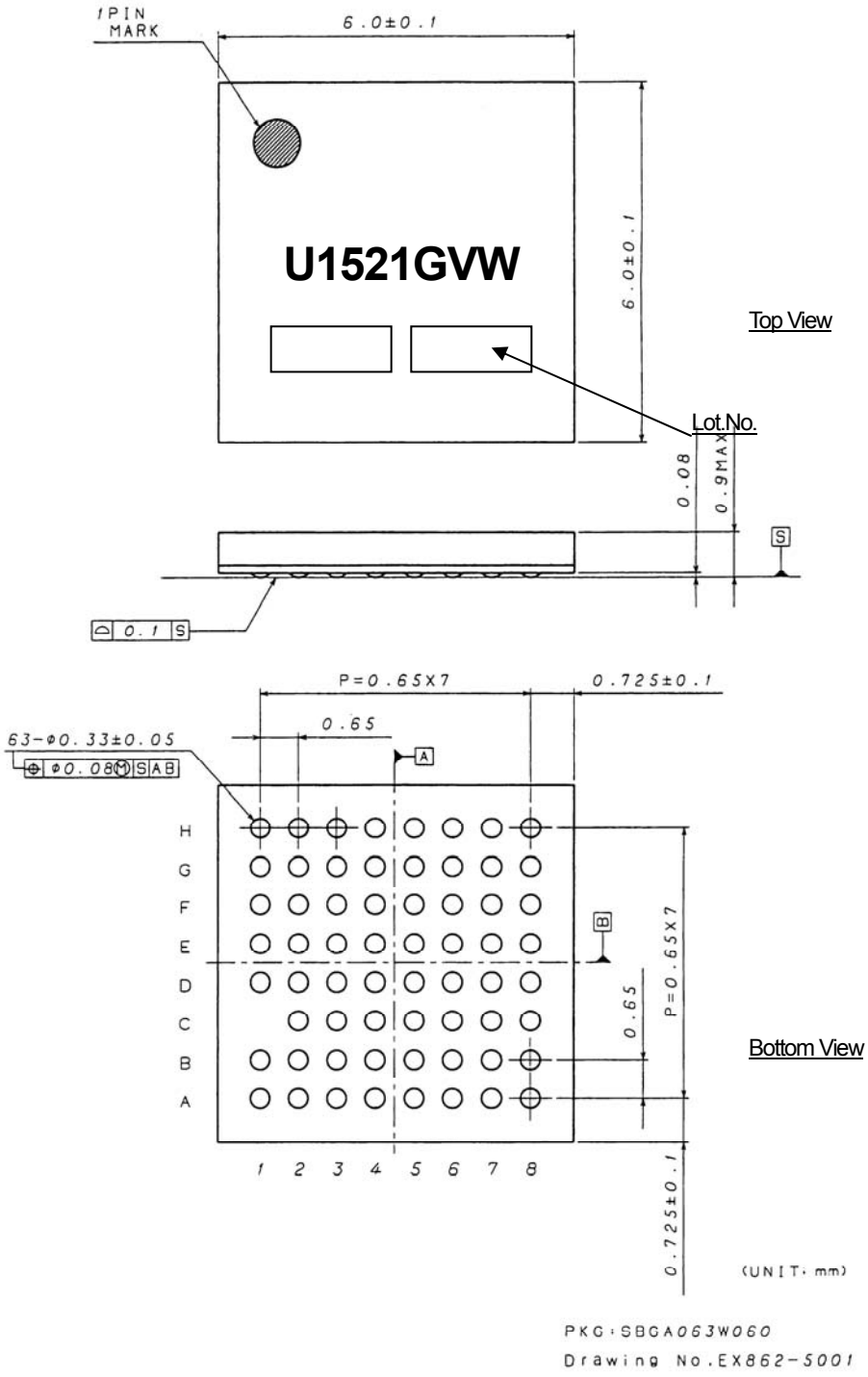


Fig. 11 BU1521GVW Package external view (SBGA063W060)

● Ordering part number

B	U	1	5	2	1	G	V	W	E	2

ROHM model name

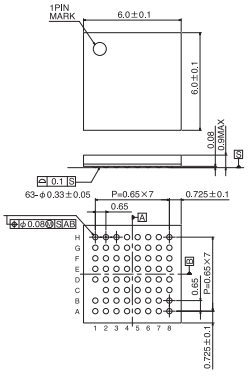
Part No.

Package
GVW: SBGA

Packaging and forming specification
E2: Embossed tape and reel

SBGA063W060

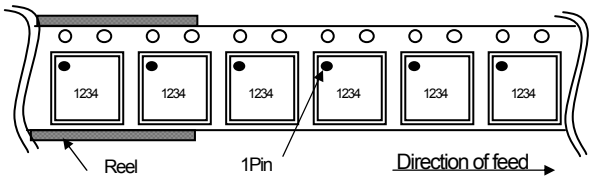
<Dimension>



(Unit:mm)

<Tape and Reel information>

Tape	Embossed carrier tape(with dry pack)
Quantity	2000pcs
Direction	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand.)



※When you order , please order in times the amount of package quantity.

Notes

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