DATA SHEET

GTL2006
13-bit GTL–/GTL/GTL+ to LVTTL translator

Product data
Supersedes data of 2003 Dec 18

2004 Jun 21

Philips
Semiconductors

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13-bit GTL–/GTL/GTL+ to LVTTL translator GTL2006

FEATURES

- Operates as a GTL–/GTL/GTL+ to LVTTL sampling receiver or LVTTL to GTL–/GTL/GTL+ driver
- 3.0 V to 3.6 V operation
- LVTTL I/O not 5 V tolerant
- Series termination on the LVTTL outputs of 30 Ω
- ESD protection exceeds 2000 V HBM per JESD22-A114, 200 V MM per JESD22-A115 and 250 V CDM per JESD22-C101
- Latch-up testing is done to JESDEC Standard JESD78 which exceeds 500 mA
- Package offered: TSSOP28

DESCRIPTION

The GTL2006 is a 13-bit translator to interface between the 3.3 V LVTTL chip set I/O and the Xeon™ processor GTL–/GTL/GTL+ I/O. The GTL2006 is designed for platform health management in dual processor applications.

PIN CONFIGURATION

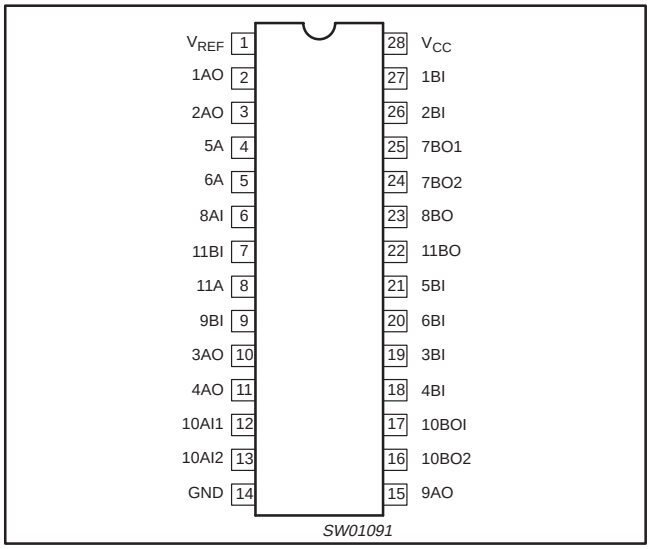


Figure 1. Pin configuration

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	V_{REF}	GTL reference voltage
2–6, 8, 10–13, 15	nAn	Data inputs/outputs (LVTTL)
7, 9, 16, 17–27	nBn	Data inputs/outputs (GTL–/GTL/GTL+)
14	GND	Ground (0 V)
28	V_{CC}	Positive supply voltage

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25 °C	TYPICAL		UNIT
			B to A	A to B	
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	C_L = 50 pF; V_{CC} = 3.3 V	5.5	5.5	ns
$C_{I/O}$	I/O pin capacitance	Outputs disabled; $V_{I/O}$ = 0 V or 3.0 V	7.8	4.5	pF

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	TOPSIDE MARK	DWG NUMBER
28-Pin Plastic TSSOP	–40 °C to +85 °C	GTL2006PW	GTL2006	SOT361-1

Standard packing quantities and other packaging data are available at www.philipslogic.com/packaging.

FUNCTION TABLES

INPUT	OUTPUT
1BI/2BI/3BI/4BI/9BI	**1AO/2AO/3AO/4AO/9AO**
L	L
H	H

INPUT	OUTPUT
8AI	**8BO**
L	L
H	H

INPUT	INPUT	OUTPUT
10AI1/10AI2	**9BI**	**10BO1/10BO2**
L	L	L
L	H	L
H	L	L
H	H	H

INPUT	INPUT/OUTPUT	OUTPUT
5BI/6BI	**5A/6A (OPEN DRAIN)**	**7BO1/7BO2**
L	L	H[1]
H	L[2]	L
H	H	H

INPUT	INPUT/OUTPUT	OUTPUT
11BI	**11A (OPEN DRAIN)**	**11BO**
L	H	L
L	L[2]	H
H	L	H

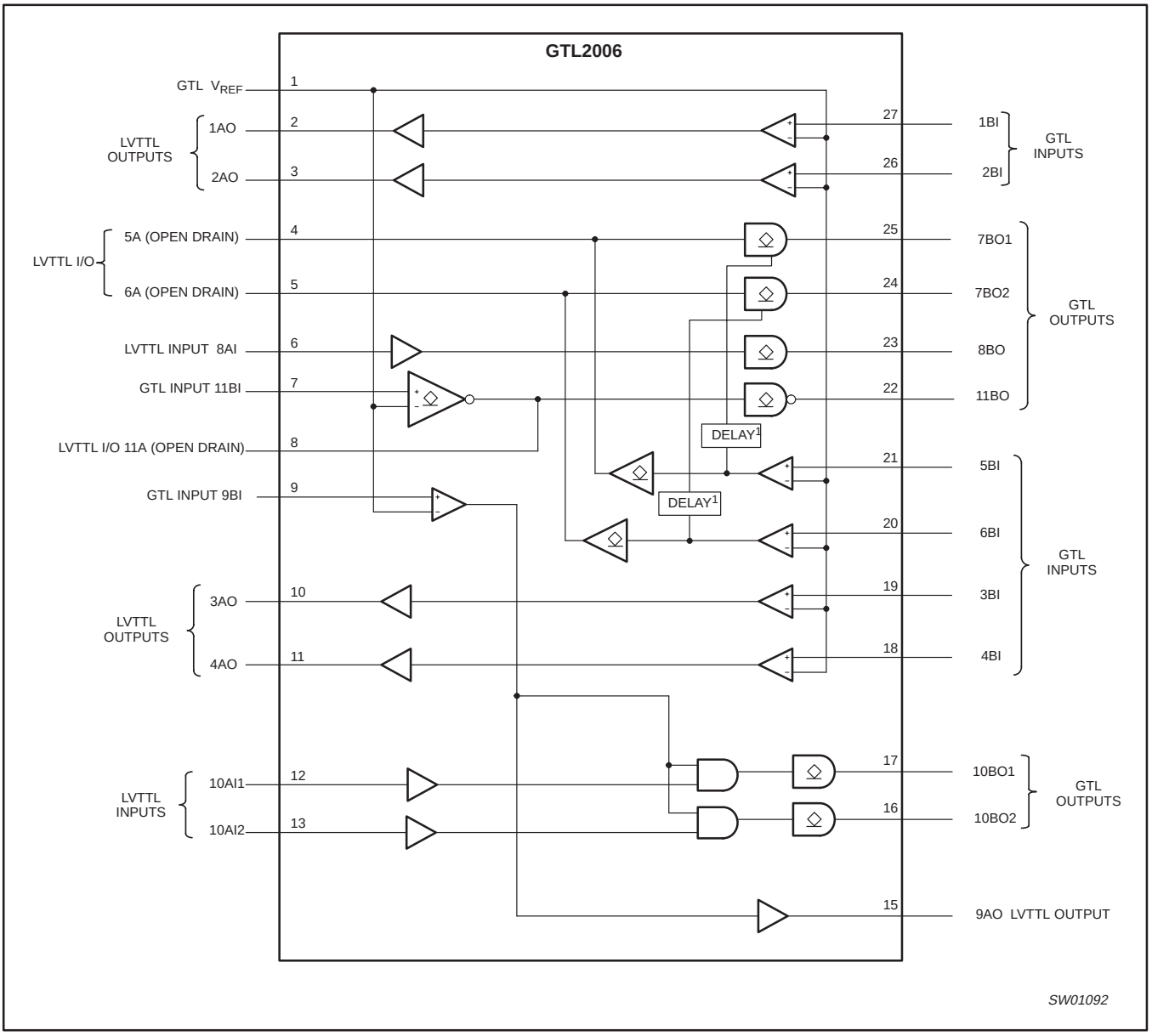
H = HIGH voltage level

L = LOW voltage level

NOTES:

1. The enable on 7BO1/7BO2 include a delay that prevents the transient condition where 5BI/6BI go from LOW to HIGH, and the LOW to HIGH on 5A/6A lags up to 100 ns from causing a low glitch on the 7BO1/7BO2 outputs.
2. Open Drain Input/Output terminal is driven to logic LOW state by other driver.

LOGIC SYMBOL



NOTE:

1. The enable on 7BO1/7BO2 include a delay that prevents the transient condition where 5BI/6BI go from LOW to HIGH, and the LOW to HIGH on 5A/6A lags up to 100 ns from causing a low glitch on the 7BO1/7BO2 outputs.

Figure 2. Logic symbol

APPLICATION INFORMATION

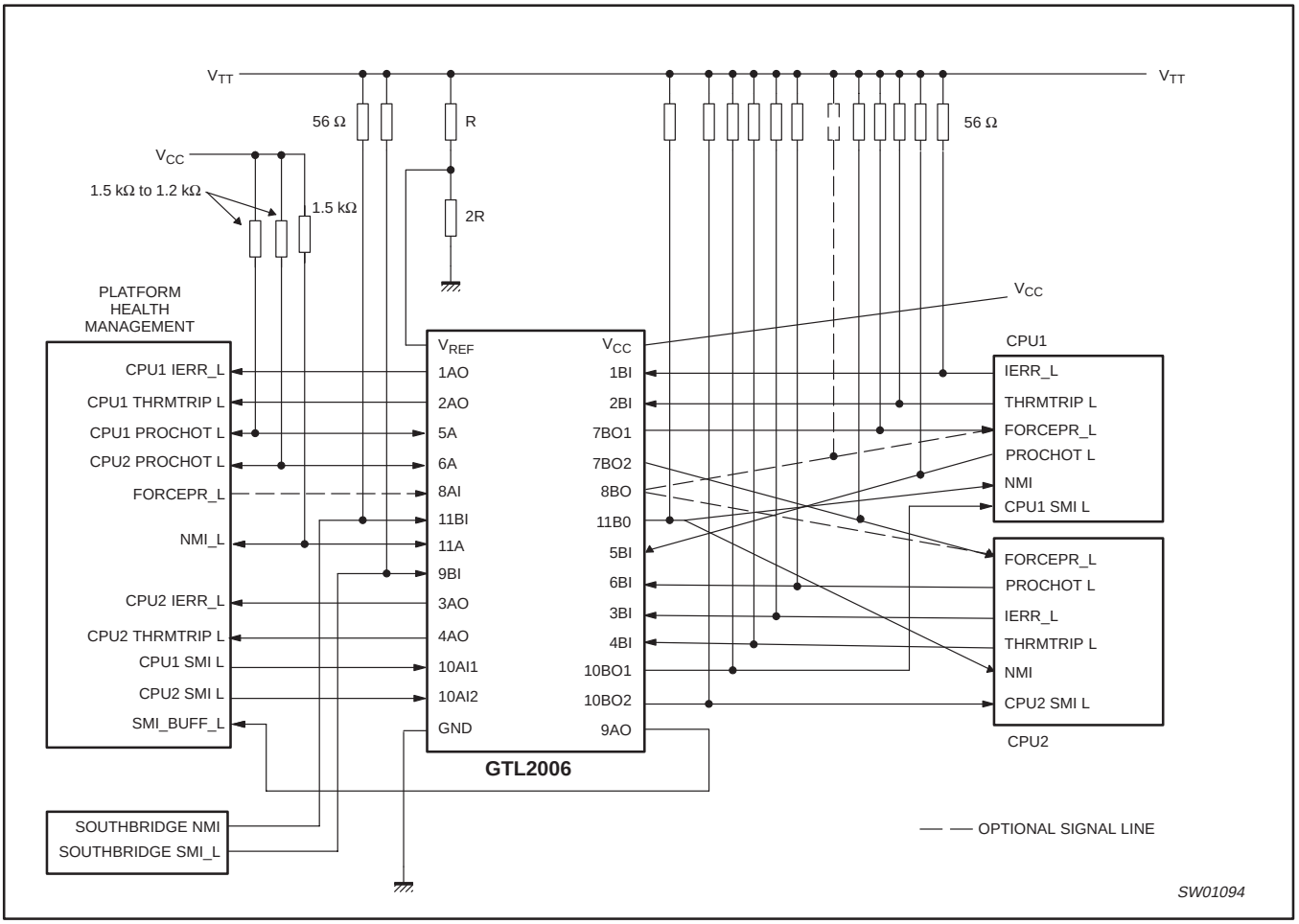


Figure 3. Application diagram

Frequently Asked Questions

Question 1: On the GTL2006 LVTTL inputs, specifically 10AI1 and 10AI2, when the GTL2006 is unpowered, these inputs may be pulled up to 3.3 V S/B and we want to make sure that there is no leakage path to the power rail under this condition. Are the LVTTL inputs HIGH Impedance when the device is unpowered and will there be any leakage?
Answer 1: When the device is unpowered, the LVTTL inputs will be in a high-impedance state and will not leak to V_{DD} if they are pulled high while the device is unpowered.

Question 2: Do all the LVTTL inputs have the same unpowered characteristic?
Answer 2: Yes.

Question 3: What is the condition of the other GTL I/O and LVTTL output pins when the device is unpowered?
Answer 3: The open drain outputs, both GTL and LVTTL, will not leak to the power supply if they are pulled high while the device is unpowered. The GTL inputs will also not leak to the power supply under the same conditions. The LVTTL totem pole outputs, however, are not open drain type outputs and there will be current flow on these pins if they are pulled high when V_{DD} is at ground.

Question 4: When this sequence occurs:
1) Pin 11BI is driven LOW (at time t0)
2) Pin 11A is driven LOW (at time t1)
3) Pin 11BI stops driving LOW (at time t2)
4)Pin 11A stops driving LOW (at time t3)
Are there wired-OR glitches at pin 11BO at time t1 and t2?
Answer 4: The output of 11BI is physically wired to the 11A pin. There will be no glitch at t1 when the external driver turns on and drives LOW, unless the external driver is a long distance away and the pull-up is a low value. If the pull-up R = Z_O of the line and the current were equally shared, the bounce would be to $^1/_2$ the pull-up voltage, presumably V_{DD}. The input is a $^1/_2$ V_{DD} threshold input, so the glitch may propagate to the 11BO. If the glitch is very short it may not propagate, or if the pull-up were higher the amplitude would be too small to propagate, or if the external driver were sinking more than half of the total current, it would not propagate. If the external driver is weak and a long way away you will most likely see a glitch on 11BO, because there will be a large glitch on 11A.

Question 5: Can you give us some guideline on how high the pull-up resistor value at pin 11A needs to be to avoid glitches on 11BO?
Answer 5: The 11A pin is a TTL pin, generally the pull-up resistor used on TTL pins are chosen to minimize power rather than to match the line impedance. Most line impedances are in the range of 50 Ω. If the pull-up is $3 \times Z_O$, that is 150 Ω; even if all the current is being sunk by the GTL2006, the initial bounce on 11A would only be $^1/_3$ V_{DD}, and would only last for the round trip time to the external driver, provided that the external driver can sink all of the current, the bounce will return LOW. The $^1/_3$ V_{DD} is not a high level to the GTL2006 11A pin, so no bounce would show up on the 11BO pin. Normal choices for the pull-up on 11A would be in the 1 kΩ to several kΩ range, depending on speed and current considerations.

Question 6: Please explain the timing specification of Bn to Bn in the AC Characteristics table. Which specific inputs/outputs does it cover, and why is the H > L transition so slow?
Answer 6: The Bn to Bn refers to the 4BI to 7BO1 path and to the 6BI to 7BO2 path. The times are disable and enable times since a LOW on 5BI or 6BI should not be reflected as a LOW on 7BO1 or 7BO2.

The t_{PLH} corresponds to the disable time, and the t_{PHL} corresponds to the enable time. The enable time is deliberately slow to prevent glitches/false LOWs on the 7BOn outputs, because a LOW on 5BI drives a LOW on 5A, which is an open-drain I/O and may have a slow rise time. And a LOW on 6BI drives a LOW on 6A that is an open-drain I/O that may also have a slow rise time.

Question 6A: Now that I try to examine the circuit from the data sheet, I am just a little bit concerned. Let me try to describe the function first:

This circuit is used for monitoring and driving the CPU PROCHOT#.

The monitor device is a Heceta7 part and its output is bi-directional, CPU1_PROCHOT# and is connected to 5A.

The CPU has an output called PROCHOT#, which goes to 5BI and an input call FRCPROCHOT# that comes from 7BO1.

When the CPU is generating PROCHPT# (5BI), we do not want the CPU input FRCPROCHOT# (7BO1) to also see this signal.

Scenario 1: CPU driving PROCHOT#
– 5BI input is HIGH and goes LOW; output 5A is HIGH and goes LOW following 5BI. The output 7BO should stay HIGH.
– 5BI input is LOW and goes HIGH; output 5A is LOW and goes HIGH following 5BI. The output 7BO1 should stay HIGH.

Scenario 2: Heceta7 driving CPU1_PROCHOT#
– 5A input is HIGH and goes LOW; output 7BO1 is HIGH and goes LOW following 5A. The input 5BI should stay HIGH.
– 5A input is LOW and goes HIGH; output 7BO1 is LOW and goes HIGH following 5A. The output 5BI should stay HIGH.

Now I can see the reason for the delay in the enable path so that we keep the output disabled to account for the potentially slow riser time on 5A. In my mind, there should also be a delay block shown in the path 5BI to 5A so that the 5BI H-to-L can disable the driver for 7BO1 before the signal appears on the 5A input/output, thus appearing as an input to the driver for 7BO1.

Have you characterized what sort of glitch you get on the 7BO1 output on an H-to-L transition on 5BI?
Answer 6A: The disable for 7BO1 comes directly from the internal 5BI signal, and by design it always disables the LOW on 7BO1 before the LOW on the 5BI can propagate to the 5AI/O and back to the 7BO1.

Question 7: Can I operate the GTL2006 at V_{TT} of 1.2 V and V_{REF} of 0.6 V?
Answer 7: Yes; you can operate V_{TT} up to 3.6 V and V_{REF} between 0.5 V to 1.8 V at any V_{TT} to adjust the high and low noise margins to your application. You don't have to follow the GTL–/GTL/GTL+ specifications. The GTL V_{IL} and V_{IH} will be 50 mV around V_{REF} within the range of 0.5 V to 1.8 V.

ABSOLUTE MAXIMUM RATINGS[1]

In accordance with the Absolute Maximum System (IEC 134); voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$ V	–50	mA
V_I	DC input voltage[3]	A port (LVTTL)	–0.5 to +4.6	V
		B port(GTL)	–0.5 to +4.6	V
I_{OK}	DC output diode current	$V_O < 0$ V	–50	mA
V_O	DC output voltage[3]	Output in Off or HIGH state; A port	–0.5 to +4.6	V
		Output in Off or HIGH state; B port	–0.5 to +4.6	V
I_{OL}	Current into any output in the LOW state	A port	32	mA
		B port	30	mA
I_{OH}	Current into any output in the HIGH state	A port	–32	mA
T_{stg}	Storage temperature range		–60 to +150	°C
$T_{J(MAX)}$	Maximum junction temperature		+125	°C

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “Recommended Operating Conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage		3.0	3.3	3.6	V
V_{TT}	Termination voltage	GTL–	0.85	0.9	0.95	V
		GTL	1.14	1.2	1.26	
		GTL+	1.35	1.5	1.65	
V_{REF}	Supply voltage	Overall	0.5	$^2/_3V_{TT}$	1.8	V
		GTL–	0.5	0.6	0.63	
		GTL	0.76	0.8	0.84	
		GTL+	0.87	1.0	1.10	
V_I	Input voltage	A port	0	3.3	3.6	V
		B port	0	V_{TT}	3.6	
V_{IH}	HIGH-level input voltage	A port	2	—	—	V
		B port	V_{REF} + 50 mV	—	—	
V_{IL}	LOW-level input voltage	A port	—	—	0.8	V
		B port	—	—	V_{REF} – 50 mV	
I_{OH}	HIGH-level output current	A port	—	—	–16	mA
I_{OL}	LOW-level output current	A port	—	—	16	mA
		B port	—	—	15	mA
T_{amb}	Operating free-air temperature range		–40	—	85	°C

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			–40 °C to +85 °C			
			MIN	TYP[1]	MAX	
V_{OH}	A port	V_{CC} = 3.0 V to 3.6 V; I_{OH} = –100 μA	V_{CC}–0.2	—	—	V
		V_{CC} = 3.0 V; I_{OH} = –16 mA	2.1	—	—	
V_{OL}	A port	V_{CC} = 3.0 V; I_{OL} = 16 mA	—	—	0.8	V
	B port	V_{CC} = 3.0 V; I_{OL} = 15 mA	—	—	0.4	
I_I	A port	V_{CC} = 3.6 V; V_I = V_{CC}	—	—	± 1	μA
		V_{CC} = 3.6 V; V_I = 0 V	—	—	± 1	
	B port	V_{CC} = 3.6 V; V_I = V_{TT} or GND	—	—	± 1	
I_{CC}	A or B port	V_{CC} = 3.6 V;V_I = V_{CC} or GND; I_O = 0 mA	—	—	12	mA
ΔI_{CC}[3]	A port or control inputs	V_{CC} = 3.6 V; V_I = V_{CC} – 0.6 V	—	—	500	μA
C_{IO}	A port	V_O = 3.0 V or 0 V	—	7.8	—	pF
	B port	V_O = V_{TT} or 0 V	—	4.5	—	

NOTES:
1. All typical values are measured at V_{CC} = 3.3 V and T_{amb} = 25 °C.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
3. This is the increase in supply current for each input that is at the specified LVTTL voltage level rather than V_{CC} or GND.

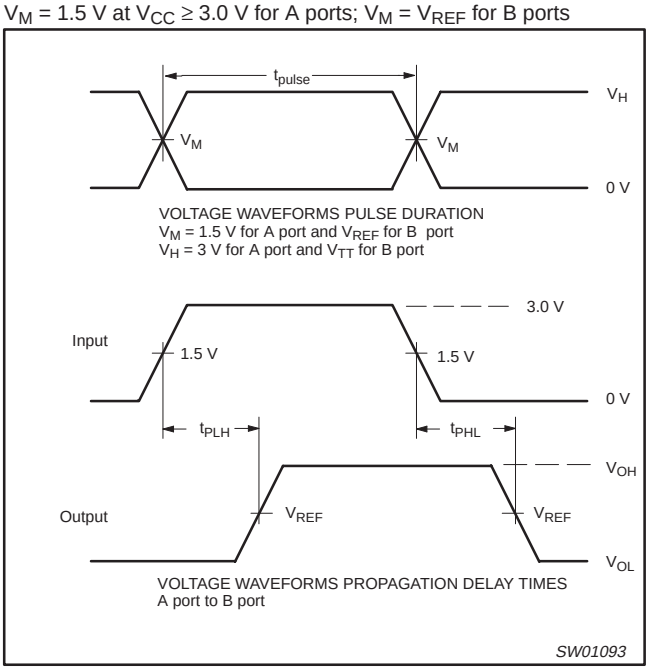
AC CHARACTERISTICS (3.3 V ± 0.3 V RANGE)

SYMBOL	PARAMETER	WAVEFORM	LIMITS (GTL–)			LIMITS (GTL)			LIMITS (GTL+)			UNIT
			V_{CC} = 3.3 V ± 0.3 V V_{REF} = 0.6 V			V_{CC} = 3.3 V ± 0.3 V V_{REF} = 0.8 V			V_{CC} = 3.3 V ± 0.3 V V_{REF} = 1.0 V			
			MIN	TYP[1]	MAX	MIN	TYP[1]	MAX	MIN	TYP[1]	MAX	
t_{PLH} t_{PHL}	An to Bn	1	2 2	4 5.5	8 10	2 2	4 5.5	8 10	2 2	4 5.5	8 10	ns
t_{PLH} t_{PHL}	Bn to An	2	2 2	5.5 5.5	10 10	2 2	5.5 5.5	10 10	2 2	5.5 5.5	10 10	ns
t_{PLH} t_{PHL}	9BI to 10BOn		2 2	6 6	11 11	2 2	6 6	11 11	2 2	6 6	11 11	ns
t_{PLH} t_{PHL}[2]	11BI to 11BO		2 2	8 14	13 21	2 2	8 14	13 21	2 2	8 14	13 21	ns
t_{PLZ} t_{PZH}	Bn to An (I/O)	3	2 2	5 5	10 10	2 2	5 5	10 10	2 2	5 5	10 10	ns
t_{PLH} t_{PHL}	Bn to Bn	3	4 120	7 205	11 350	4 120	7 205	11 350	4 120	7 205	11 350	ns

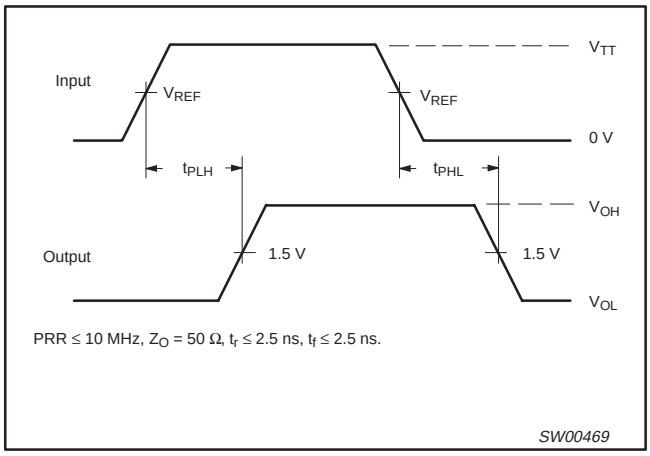
NOTES:
1. All typical values are at V_{CC} = 3.3 V and T_{amb} = 25 °C.
2. Includes ~7.6 ns RC rise time of test load pull-up on 11A, 1.5 kΩ pull-up and 21 pF load on 11A has about 23 ns RC rise time.

AC WAVEFORMS

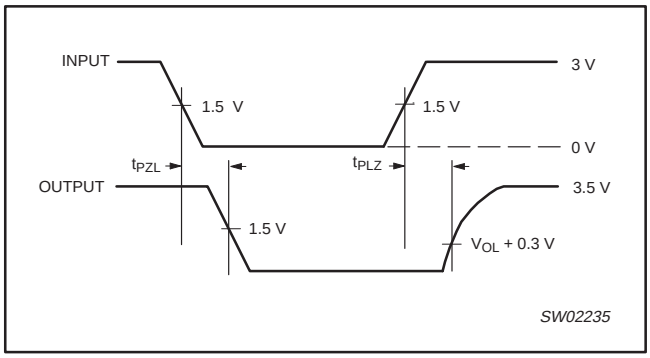
V_M = 1.5 V at $V_{CC} \geq$ 3.0 V for A ports; $V_M = V_{REF}$ for B ports



Waveform 1.

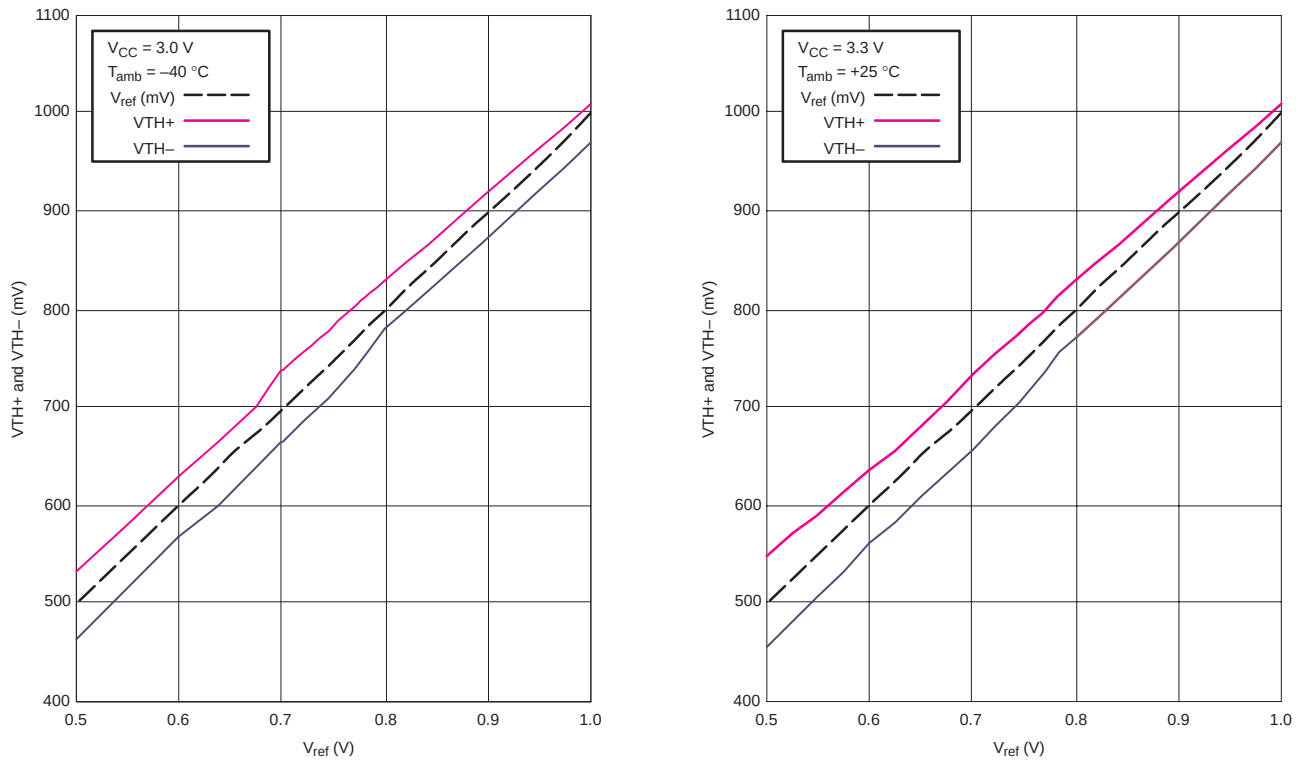


Waveform 2.



Waveform 3.

PERFORMANCE CURVES



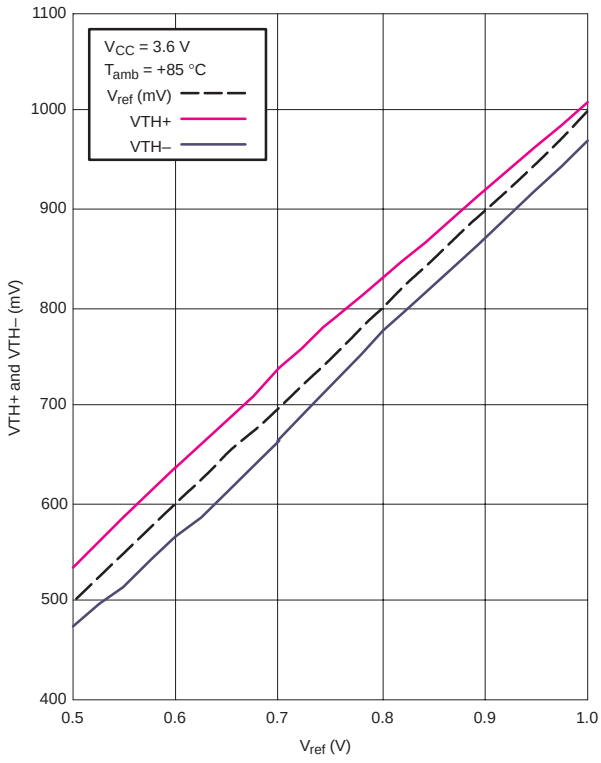


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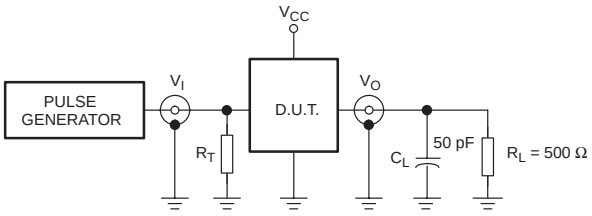
Figure 4. GTL V_{TH+} and V_{TH-} versus V_{REF}

TEST CIRCUIT



Test circuit for switching times

DEFINITIONS

R_L = Load resistor

C_L = Load capacitance includes jig and probe capacitance

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

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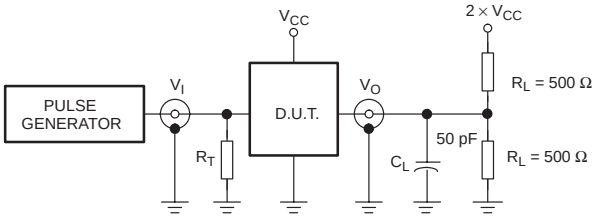
Figure 5. Load circuitry for A outputs



Test Circuit for open drain LVTTL I/O

DEFINITIONS

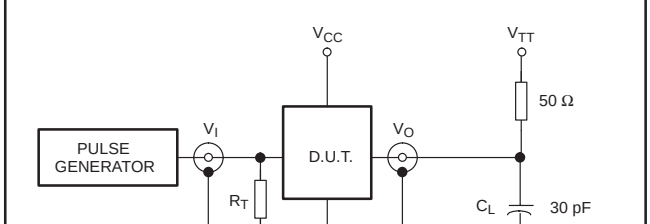
R_L = Load resistor

C_L = Load capacitance includes jig and probe capacitance

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

SW02067

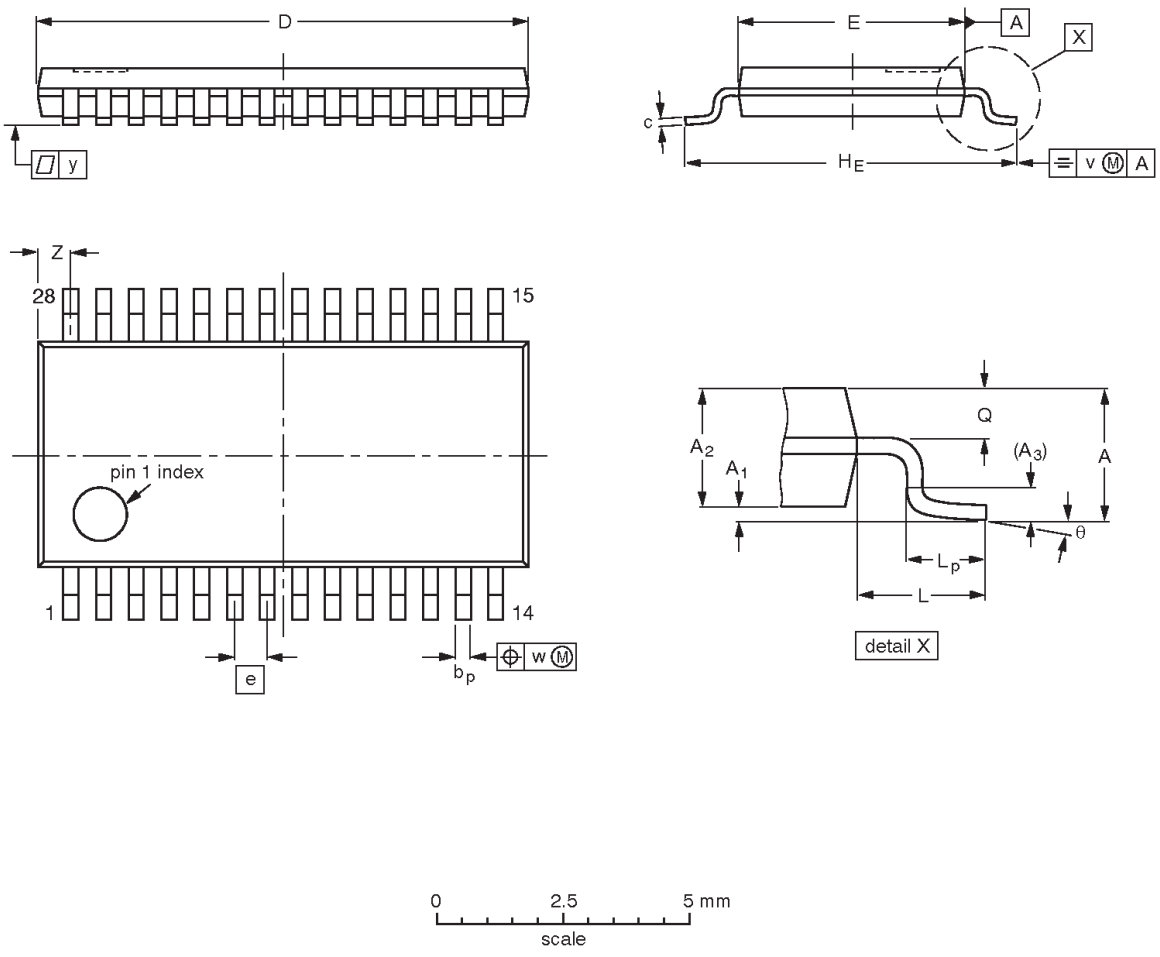
Figure 6. Load circuitry for open drain LVTTL I/O



SW02066

Figure 7. Load circuit for B outputs

TSSOP28: plastic thin shrink small outline package; 28 leads; body width 4.4 mm **SOT361-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	9.8 9.6	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.8 0.5	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT361-1		MO-153				~~99-12-27~~ 03-02-19

REVISION HISTORY

Rev	Date	Description
_2	20040621	**Product data (9397 750 13063). Supersedes data of 2003 Dec 18.** Modifications: ● All figures numbered. ● Figure 2, “Logic symbol” modified. ● Page 6, Frequently asked Questions: add questions/answers 4, 5, 6, 6A, and 7. ● Page 8, AC Characteristics (3.3 V ± 0.3 Range); t_{PHL} An to Bn, GTL+ maximum: change from ‘1. ns’ to ‘10 ns’. ● Add “Performance curves” section on page 10.
_1	20031218	**Product data (9397 750 12562); ECN 853-2440 01-A14985 dated 15 December 2003.**

Data sheet status

Level	Data sheet status [1]	Product status [2] [3]	Definitions
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
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[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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