

RF Power Field Effect Transistors

N-Channel Enhancement-Mode Lateral MOSFETs

Designed for PCN and PCS base station applications with frequencies from 2000 to 2200 MHz. Suitable for FM, TDMA, CDMA and multicarrier amplifier applications. To be used in Class AB for PCN-PCS/cellular radio and WLL applications.

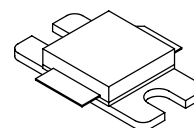
- Wideband CDMA Performance: -45 dB ACPR @ 4.096 MHz, 28 Volts Output Power — 3.5 Watts
 Power Gain — 14 dB
 Efficiency — 15%
- Capable of Handling 10:1 VSWR, @ 28 Vdc, 2110 MHz, 30 Watts CW Output Power

Features

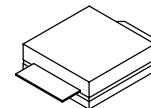
- High Gain, High Efficiency and High Linearity
- Integrated ESD Protection
- Designed for Maximum Gain and Insertion Phase Flatness
- Excellent Thermal Stability
- Characterized with Series Equivalent Large-Signal Impedance Parameters
- Low Gold Plating Thickness on Leads, 40μ" Nominal.
- RoHS Compliant
- In Tape and Reel. R3 Suffix = 250 Units per 32 mm, 13 Inch Reel.

MRF21030LR3
MRF21030LSR3

2200 MHz, 30 W, 28 V
LATERAL N-CHANNEL
RF POWER MOSFETs



CASE 465E-04, STYLE 1
NI-400
MRF21030LR3



CASE 465F-04, STYLE 1
NI-400S
MRF21030LSR3

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Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V _{DSS}	-0.5, +65	Vdc
Gate-Source Voltage	V _{GS}	-0.5, +15	Vdc
Total Device Dissipation @ T _C = 25°C Derate above 25°C	P _D	83.3 0.48	W W/°C
Storage Temperature Range	T _{stg}	- 65 to +150	°C
Case Operating Temperature	T _C	150	°C
Operating Junction Temperature	T _J	200	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case	R _{θJC}	2.1	°C/W

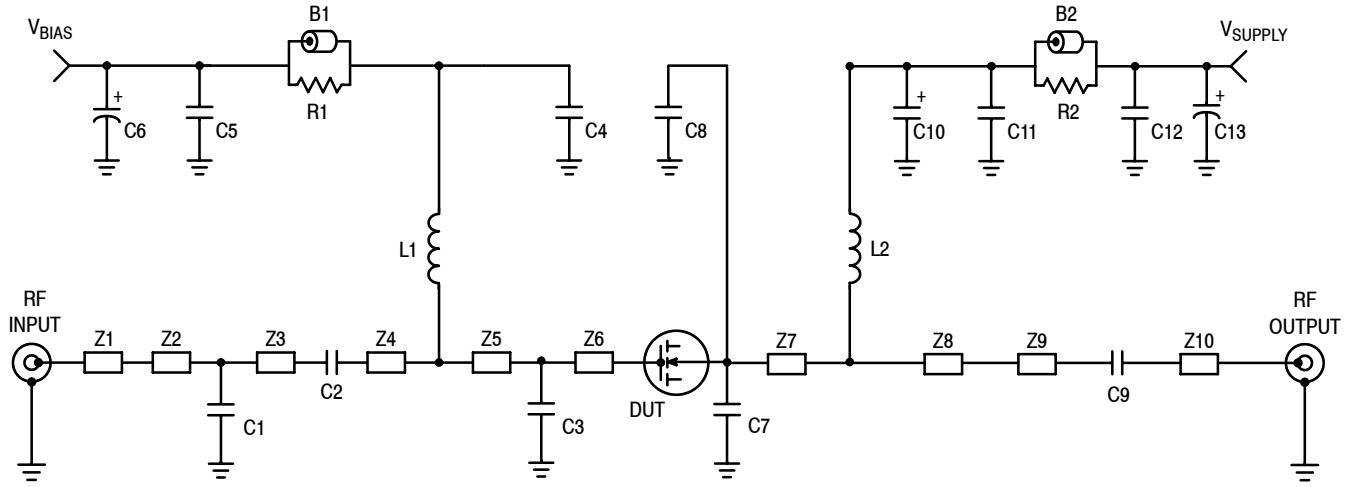
Table 3. ESD Protection Characteristics

Test Conditions	Class
Human Body Model	2 (Minimum)
Machine Model	M3 (Minimum)

Table 4. Electrical Characteristics ($T_C = 25^\circ\text{C}$ unless otherwise noted)

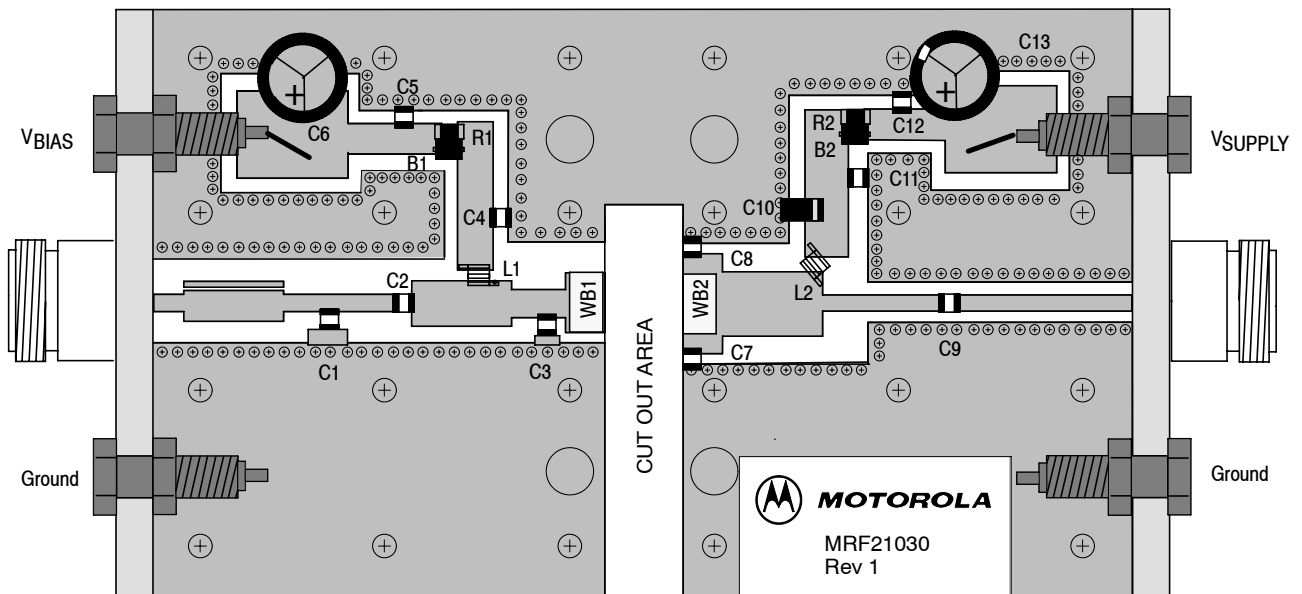
Characteristic	Symbol	Min	Typ	Max	Unit
Off Characteristics					
Drain-Source Breakdown Voltage ($V_{GS} = 0\text{ Vdc}$, $I_D = 20\ \mu\text{A}$)	$V_{(BR)DSS}$	65	—	—	Vdc
Zero Gate Voltage Drain Current ($V_{DS} = 28\text{ Vdc}$, $V_{GS} = 0\text{ Vdc}$)	I_{DSS}	—	—	1	μAdc
Gate-Source Leakage Current ($V_{GS} = 5\text{ Vdc}$, $V_{DS} = 0\text{ Vdc}$)	I_{GSS}	—	—	1	μAdc
On Characteristics					
Gate Threshold Voltage ($V_{DS} = 10\text{ Vdc}$, $I_D = 100\ \mu\text{Adc}$)	$V_{GS(th)}$	2	3	4	Vdc
Gate Quiescent Voltage ($V_{DS} = 28\text{ Vdc}$, $I_D = 250\text{ mA}$)	$V_{GS(Q)}$	2	3.3	4.5	Vdc
Drain-Source On-Voltage ($V_{GS} = 10\text{ Vdc}$, $I_D = 1\text{ Adc}$)	$V_{DS(on)}$	—	0.29	0.4	Vdc
Forward Transconductance ($V_{DS} = 10\text{ Vdc}$, $I_D = 1\text{ Adc}$)	g_{fs}	—	2	—	S
Dynamic Characteristics					
Input Capacitance (Including Input Matching Capacitor in Package) ⁽¹⁾ ($V_{DS} = 28\text{ Vdc}$, $V_{GS} = 0$, $f = 1\text{ MHz}$)	C_{iss}	—	98.5	—	pF
Output Capacitance ⁽¹⁾ ($V_{DS} = 28\text{ Vdc}$, $V_{GS} = 0$, $f = 1\text{ MHz}$)	C_{oss}	—	37	—	pF
Reverse Transfer Capacitance ($V_{DS} = 28\text{ Vdc}$, $V_{GS} = 0$, $f = 1\text{ MHz}$)	C_{rss}	—	1.3	—	pF
Functional Tests (In Freescale Test Fixture, 50 ohm system)					
Two-Tone Common-Source Amplifier Power Gain ($V_{DD} = 28\text{ Vdc}$, $P_{out} = 30\text{ W PEP}$, $I_{DQ} = 250\text{ mA}$, $f_1 = 2140.0\text{ MHz}$, $f_2 = 2140.1\text{ MHz}$)	G_{ps}	—	13	—	dB
Two-Tone Drain Efficiency ($V_{DD} = 28\text{ Vdc}$, $P_{out} = 30\text{ W PEP}$, $I_{DQ} = 250\text{ mA}$, $f_1 = 2140.0\text{ MHz}$, $f_2 = 2140.1\text{ MHz}$)	η	—	33	—	%
3rd Order Intermodulation Distortion ($V_{DD} = 28\text{ Vdc}$, $P_{out} = 30\text{ W PEP}$, $I_{DQ} = 250\text{ mA}$, $f_1 = 2140.0\text{ MHz}$, $f_2 = 2140.1\text{ MHz}$)	IMD	—	-30	—	dBc
Input Return Loss ($V_{DD} = 28\text{ Vdc}$, $P_{out} = 30\text{ W PEP}$, $I_{DQ} = 250\text{ mA}$, $f_1 = 2140.0\text{ MHz}$, $f_2 = 2140.1\text{ MHz}$)	IRL	—	-13	—	dB
Two-Tone Common-Source Amplifier Power Gain ($V_{DD} = 28\text{ Vdc}$, $P_{out} = 30\text{ W PEP}$, $I_{DQ} = 250\text{ mA}$, $f_1 = 2110.0\text{ MHz}$, $f_2 = 2110.1\text{ MHz}$ and $f_1 = 2170.0\text{ MHz}$, $f_2 = 2170.1\text{ MHz}$)	G_{ps}	12	13	—	dB
Two-Tone Drain Efficiency ($V_{DD} = 28\text{ Vdc}$, $P_{out} = 30\text{ W PEP}$, $I_{DQ} = 250\text{ mA}$, $f_1 = 2110.0\text{ MHz}$, $f_2 = 2110.1\text{ MHz}$ and $f_1 = 2170.0\text{ MHz}$, $f_2 = 2170.1\text{ MHz}$)	η	31	33	—	%
3rd Order Intermodulation Distortion ($V_{DD} = 28\text{ Vdc}$, $P_{out} = 30\text{ W PEP}$, $I_{DQ} = 250\text{ mA}$, $f_1 = 2110.0\text{ MHz}$, $f_2 = 2110.1\text{ MHz}$ and $f_1 = 2170.0\text{ MHz}$, $f_2 = 2170.1\text{ MHz}$)	IMD	—	-30	-27.5	dBc
Input Return Loss ($V_{DD} = 28\text{ Vdc}$, $P_{out} = 30\text{ W PEP}$, $I_{DQ} = 250\text{ mA}$, $f_1 = 2110.0\text{ MHz}$, $f_2 = 2110.1\text{ MHz}$ and $f_1 = 2170.0\text{ MHz}$, $f_2 = 2170.1\text{ MHz}$)	IRL	—	-13	-9	dB

1. Part is internally matched both on input and output.



B1, B2	Short Ferrite Beads	Z1	0.153" x 0.087" Microstrip
C1	1 pF Chip Capacitor	Z2	0.509" x 0.156" Microstrip
C2	4.7 pF Chip Capacitor	Z3	0.572" x 0.087" Microstrip
C3	0.5 pF Chip Capacitor	Z4	0.509" x 0.232" Microstrip
C4	3.9 pF Chip Capacitor	Z5	0.277" x 0.143" Microstrip
C5, C12	0.1 μ F Chip Capacitors	Z6	0.200" x 0.305" Microstrip
C6, C13	470 μ F, 63 V Electrolytic Chip Capacitors	Z7	0.200" x 0.511" Microstrip
C7, C8	0.3 pF Chip Capacitors	Z8	0.510" x 0.328" Microstrip
C9	3.6 pF Chip Capacitor	Z9	0.608" x 0.081" Microstrip
C10	22 μ F Tantalum Chip Capacitor	PCB	Taconic TLX8, 30 mils, $\epsilon_r = 2.55$
C11	5.1 pF Chip Capacitor		
L1, L2	12.5 nH Inductors		
R1, R2	12 Ω Chip Resistors (1206)		

Figure 1. MRF21030LR3(SR3) Test Circuit Schematic



Freescale has begun the transition of marking Printed Circuit Boards (PCBs) with the Freescale Semiconductor signature/logo. PCBs may have either Motorola or Freescale markings during the transition period. These changes will have no impact on form, fit or function of the current product.

Figure 2. MRF21030LR3(SR3) Test Circuit Component Layout

TYPICAL CHARACTERISTICS

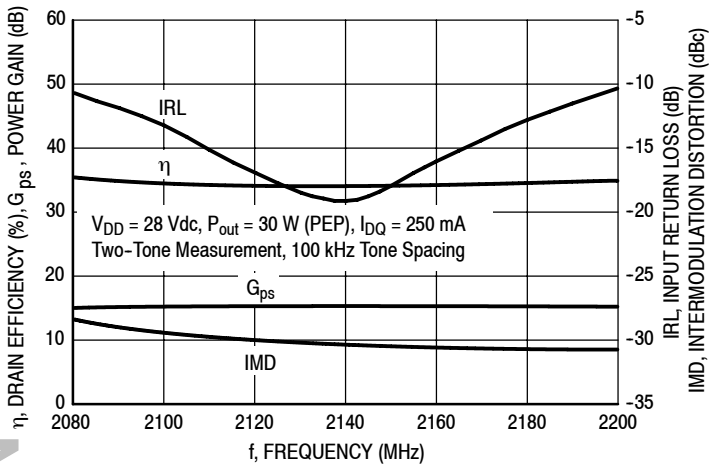


Figure 3. Class AB Broadband Circuit Performance

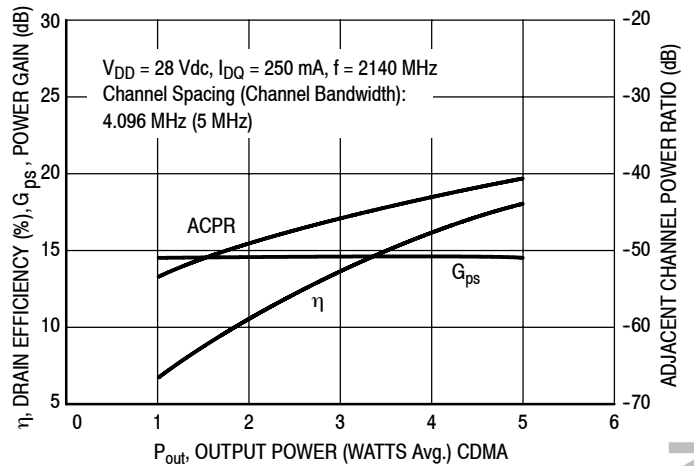


Figure 4. CDMA ACPR, Power Gain and Drain Efficiency versus Output Power

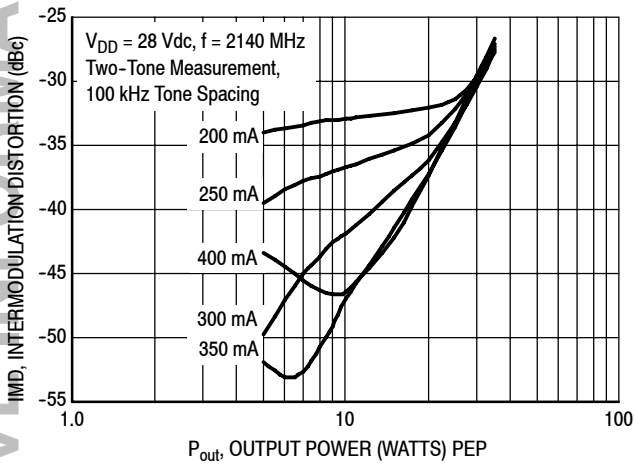


Figure 5. Intermodulation Distortion versus Output Power

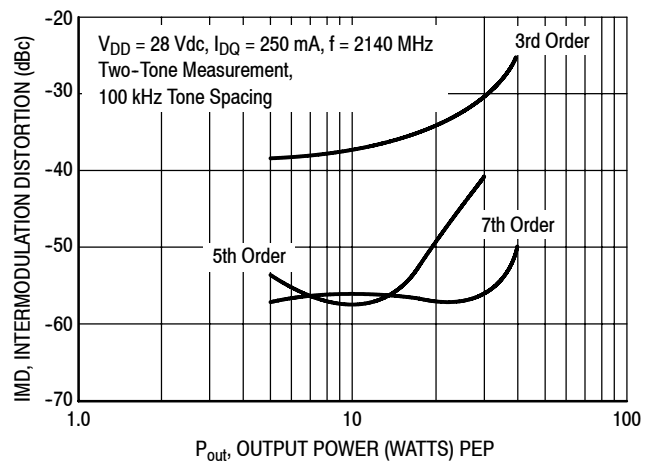


Figure 6. Intermodulation Distortion Products versus Output Power

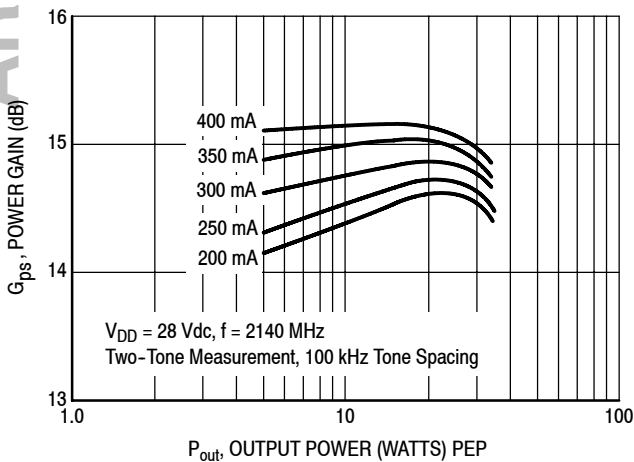


Figure 7. Power Gain versus Output Power

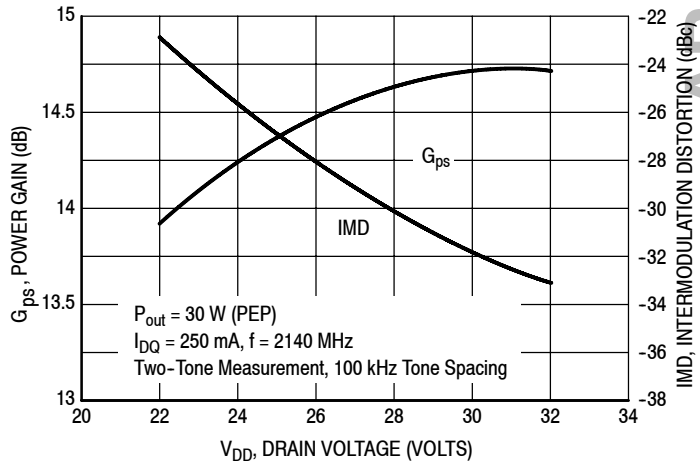
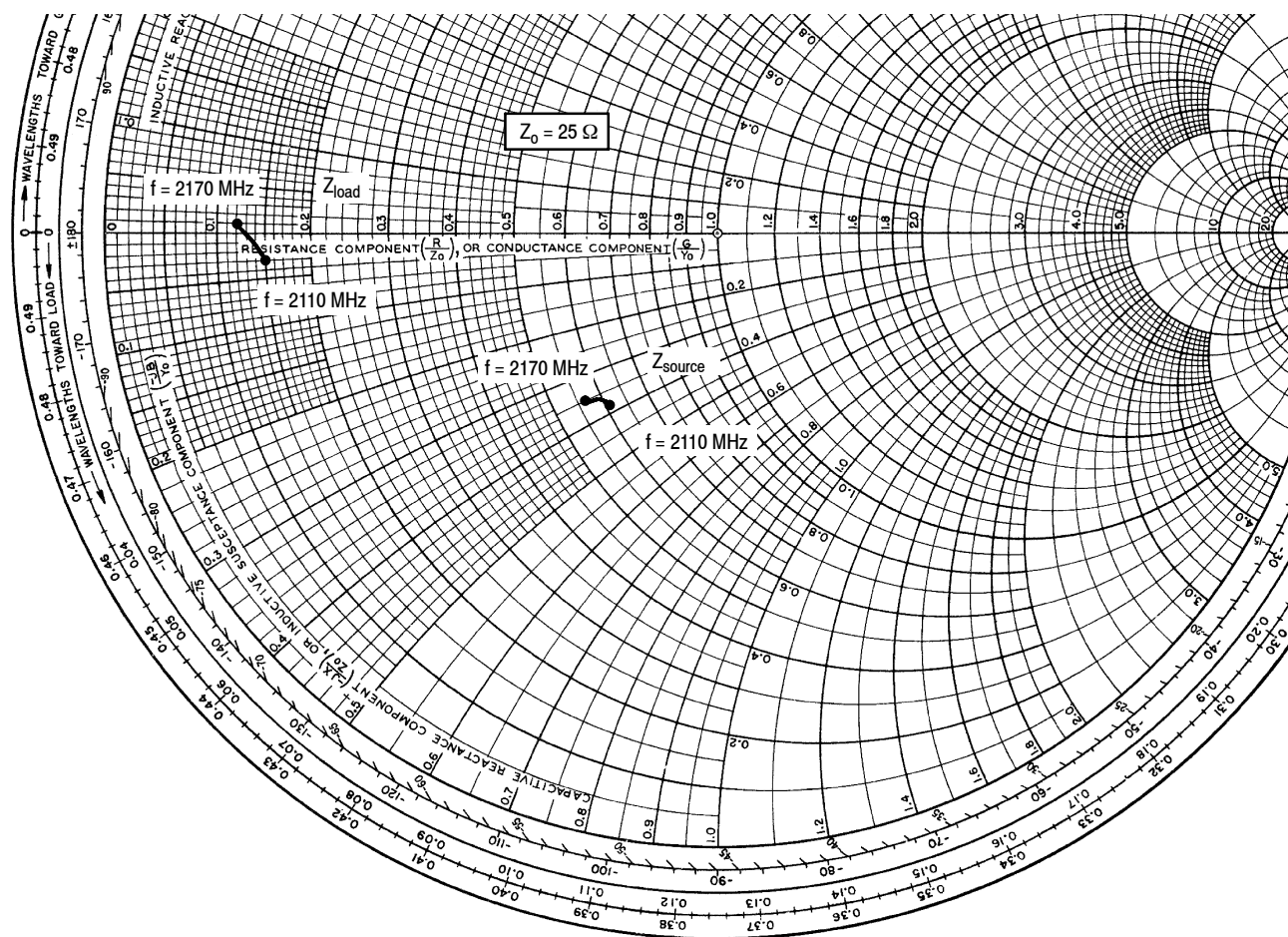


Figure 8. Power Gain and Intermodulation Distortion versus Supply Voltage



$V_{DD} = 28\text{ V}$, $I_{DQ} = 250\text{ mA}$, $P_{out} = 30\text{ W PEP}$

f MHz	Z_{source} Ω	Z_{load} Ω
2110	$15.3 - j9.4$	$3.7 - j0.78$
2140	$14.6 - j9.4$	$3.4 - j0.37$
2170	$14.3 - j8.8$	$3.0 + j0.13$

Z_{source} = Test circuit impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.

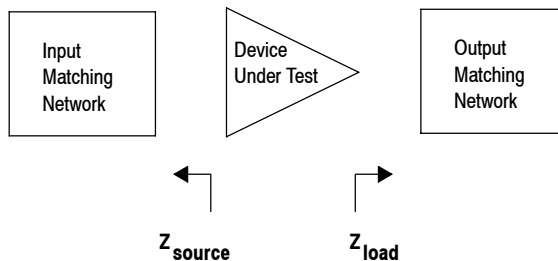
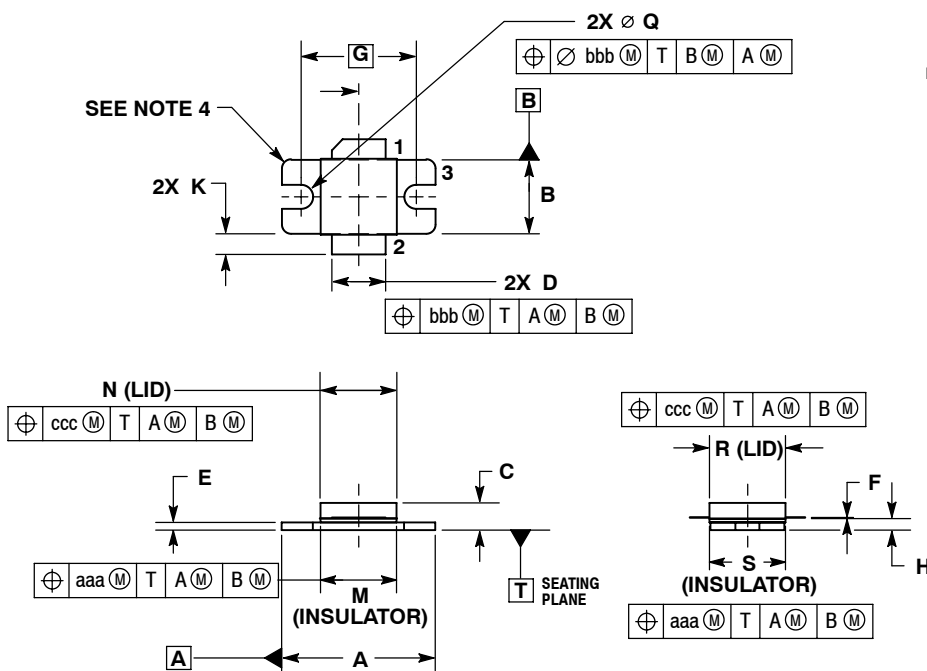


Figure 9. Series Equivalent Source and Load Impedance

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PACKAGE DIMENSIONS



NOTES:

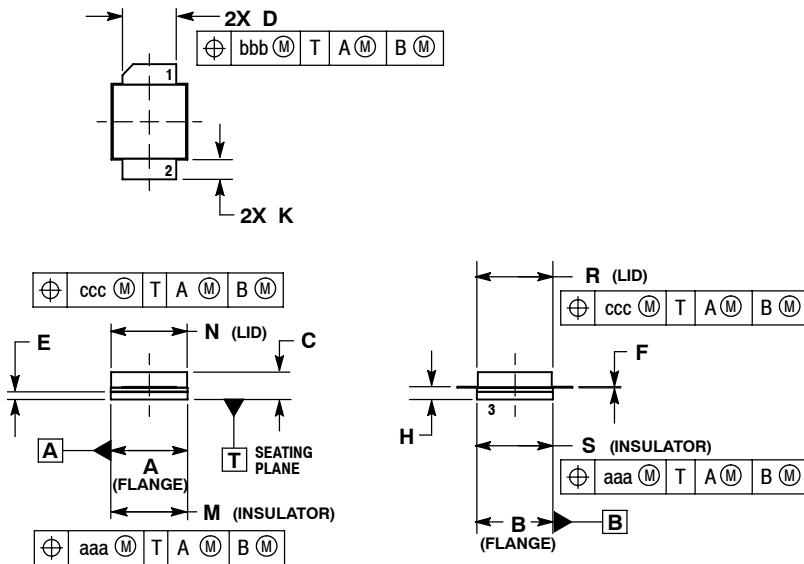
1. CONTROLLING DIMENSION: INCH.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSION H IS MEASURED 0.030 (0.762) AWAY FROM PACKAGE BODY.
4. INFORMATION ONLY: CORNER BREAK (4X) TO BE $.060 \pm .005$ (1.52 ± 0.13) RADIUS OR $.06 \pm .005$ (1.52 ± 0.13) x 45° CHAMFER.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.795	.805	20.19	20.44
B	.380	.390	9.65	9.9
C	.125	.163	3.17	4.14
D	.275	.285	6.98	7.24
E	.035	.045	0.89	1.14
F	.004	.006	0.10	0.15
G	.600 BSC		15.24 BSC	
H	.057	.067	1.45	1.7
K	.092	.122	2.33	3.1
M	.395	.405	10	10.3
N	.395	.405	10	10.3
Q	$\varnothing .120$	$\varnothing .130$	$\varnothing 3.05$	$\varnothing 3.3$
R	.395	.405	10	10.3
S	.395	.405	10	10.3
aaa	.005 BSC		0.127 BSC	
bbb	.010 BSC		0.254 BSC	
ccc	.015 BSC		0.381 BSC	

STYLE 1:

- PIN 1. DRAIN
- GATE
- SOURCE

**CASE 465E-04
ISSUE F
NI-400
MRF21030LR3**



NOTES:

1. CONTROLLING DIMENSION: INCH.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
3. DIMENSION H IS MEASURED 0.030 (0.762) AWAY FROM PACKAGE BODY.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.395	.405	10.03	10.29
B	.395	.405	10.03	10.29
C	.125	.163	3.18	4.14
D	.275	.285	6.98	7.24
E	.035	.045	0.89	1.14
F	.004	.006	0.10	0.15
H	.057	.067	1.45	1.70
K	.092	.122	2.34	3.10
M	.395	.405	10.03	10.29
N	.395	.405	10.03	10.29
R	.395	.405	10.03	10.29
S	.395	.405	10.03	10.29
aaa	.005 REF		0.127 REF	
bbb	.010 REF		0.254 REF	
ccc	.015 REF		0.38 REF	

STYLE 1:

- PIN 1. DRAIN
- GATE
- SOURCE

**CASE 465F-04
ISSUE E
NI-400S
MRF21030LSR3**

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REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
12	Dec. 2010	<ul style="list-style-type: none"> • MRF21030 Rev. 12 data sheet archived. Data sheet split due to change in part life cycle. See MRF21030-1 Rev. 13 for MRF21030LSR3 and MRF21030-2 Rev. 14 for MRF21030LR3.

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