dsPIC33FJ64MCX06A/X08A/X10A and dsPIC33FJ128MCX06A/X08A/X10A Family Silicon Errata and Data Sheet Clarification

The dsPIC33FJ64MCX06A/X08A/X10A and dsPIC33FJ128MCX06A/X08A/X10A family devices that you have received conform functionally to the current Device Data Sheet (DS70594**C**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the dsPIC33FJ64MCX06A/X08A/X10A and dsPIC33FJ128MCX06A/X08A/X10A silicon.

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**A5**).

Data Sheet clarifications and corrections start on page 10, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers and emulation tools, which are available at the Microchip corporate web site (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with MPLAB ICD 3 or PICkit™ 3:

1. Using the appropriate interface, connect the device to the MPLAB ICD 3 programmer/debugger or PICkit 3.
2. From the main menu in MPLAB IDE, select *Configure>Select Device*, and then select the target part number in the dialog box.
3. Select the MPLAB hardware tool (*Debugger>Select Tool*).
4. Perform a "Connect" operation to the device (*Debugger>Connect*). Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

Note: If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The Device and Revision ID values for the various dsPIC33FJ64MCX06A/X08A/X10A and dsPIC33FJ128MCX06A/X08A/X10A silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID(1)	Revision ID for Silicon Revision(2)		
		A3	A4	A5
dsPIC33FJ64MC506A	0x0089	0x3009	0x300A	0x300B
dsPIC33FJ64MC508A	0x008A			
dsPIC33FJ64MC510A	0x008B			
dsPIC33FJ64MC706A	0x0091			
dsPIC33FJ64MC710A	0x0097			
dsPIC33FJ128MC506A	0x00A1			
dsPIC33FJ128MC510A	0x00A3			
dsPIC33FJ128MC706A	0x00A9			
dsPIC33FJ128MC708A	0x00AE			
dsPIC33FJ128MC710A	0x00AF			

Note 1: The Device and Revision IDs (DEVID and DEVREV) are located at the last two implemented addresses in program memory.

2: Refer to the *"dsPIC33F/PIC24H Flash Programming Specification"* (DS70152) for detailed information on Device and Revision IDs for your specific device.

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TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions(1)		
				A3	A4	A5
ECAN™	Sleep Mode	1.	The WAKIF bit in the CxINTF register cannot be cleared by software instruction after the device is interrupted from Sleep due to activity on the CAN bus.	X	X	X
UART	IR Mode	2.	The 16x baud clock signal on the BCLK pin is present only when the module is transmitting.	X	X	X
UART	High-Speed Mode	3.	When the UART is in 4x mode (BRGH = 1) and using two Stop bits (STSEL = 1), it may sample the first Stop bit instead of the second one.	X	X	X
UART	Interrupts	4.	The UART error interrupt may not occur, or may occur at an incorrect time, if multiple errors occur during a short period of time.	X	X	X
I^2C™	10-bit Addressing Mode	5.	When the I^2C module is configured for 10-bit addressing using the same address bits (A10 and A9) as other I^2C devices, the A10 and A9 bits may not work as expected.	X	X	X
I^2C	—	6.	After the ACKSTAT bit is set when receiving a NACK, it may be cleared by the reception of a Start or Stop bit.	X	X	X
I^2C	10-bit Addressing Mode	7.	The 10-bit slave does not set the RBF flag or load the I2CxRCV register on address match if the Least Significant bits (LSbs) of the address are the same as the 7-bit reserved addresses.	X	X	X
I^2C	10-bit Addressing Mode	8.	When the I^2C module is configured as a 10-bit slave with an address of 0x102, the I2CxRCV register content for the lower address byte is 0x01 rather than 0x02.	X	X	X
SPI	Frame Mode	9.	In framed SPI mode, when the FRMDLY bit (SPIxCON2<1>) is cleared and SMP bit (SPIxCON1<9>) is cleared, frame sync pulses do not get generated.	X	X	X
Internal Voltage Regulator	IPD	10.	When the VREGS bit (RCON<8>) is set to a logic '0', device may Reset and higher sleep current may be observed.	X	X	X
PSV Operations	—	11.	An address error trap occurs in certain addressing modes when accessing the first four bytes of any PSV page.	X	X	X
CPU	EXCH Instruction	12.	The EXCH instruction does not execute correctly.	X	X	X
SPI	Transmit Operation	13.	Writing to the SPIxBUF register as soon as TBF bit is cleared will cause SPI module to ignore written data.	X	X	X
ECAN	Transmission Queuing	14.	ECAN module may not transmit Buffer 0 data if Buffer 1 data is queued for transmission first.	X	X	X
UART	Break Character Generation	15.	The UART module will not generate back-to-back Break characters.	X	X	X
QEI	Timer Gated Accumulation Mode	16.	When Timer Gated Accumulation is enabled, the QEI does not generate an interrupt on every falling edge.	X	X	X
QEI	Timer Gated Accumulation Mode	17.	When Timer Gated Accumulation is enabled, and an external signal is applied, the POSCNT increments and generates an interrupt after a match with MAXCNT.	X	X	X
I/O	SDO1 Pin	18.	SDO1 pin may toggle while device is being programmed via PGECx/PGEDx pin pairs.	X	X	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

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TABLE 2: SILICON ISSUE SUMMARY (CONTINUED)

Module	Feature	Item Number	Issue Summary	Affected Revisions(1)		
				A3	A4	A5
ADC	Current Consumption in Sleep Mode	19.	If the ADC module is in an enabled state when the device enters Sleep mode, the power-down current (IPD) of the device may exceed the device data sheet specifications.	X	X	X
All	150ºC Operation	20.	These revisions of silicon only support 140ºC operation instead of 150ºC for Hi-Temp operating temperature.	X	X	
Sleep Mode	Current Consumption	21.	The device power-down current (IPD) exceeds the specifications listed in the device data sheet.	X	X	
CPU	Interrupt Disable	22.	When a previous `DISI` instruction is active (i.e., the DISICNT register is non-zero), and the value of the DISICNT register is updated manually, the DISICNT register freezes and disables interrupts permanently.	X	X	X
CPU	`div.sd`	23.	When using the `div.sd` instruction, the overflow bit is not getting set when an overflow occurs.	X	X	X
UART	TX Interrupt	24.	A transmit (TX) Interrupt may occur before the data transmission is complete.	X	X	X
JTAG	Flash Programming	25.	JTAG Flash programming is not supported.	X	X	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**A5**).

1. Module: ECAN™

The WAKIF bit in the CxINTF register cannot be cleared by software instruction after the device is interrupted from Sleep due to activity on the CAN bus.

When the device wakes up from Sleep due to CAN bus activity, the ECAN module is placed in operational mode. The ECAN Event interrupt occurs due to the WAKIF flag. Trying to clear the flag in the Interrupt Service Routine (ISR) may not clear the flag. The WAKIF bit being set will not cause repetitive Interrupt Service Routine execution.

Work around

Although the WAKIF bit does not clear, the device Sleep and ECAN Wake function continue to work as expected. If the ECAN event is enabled, the CPU will enter the ISR due to the WAKIF flag getting set. The application can maintain a secondary flag, which tracks the device Sleep and Wake events.

Affected Silicon Revisions

A3	A4	A5					
X	X	X					

2. Module: UART

When the UART is configured for IR interface operations (UxMODE<9:8> = 11), the 16x baud clock signal on the BCLK pin is present only when the module is transmitting. The pin is idle at all other times.

Work around

Configure one of the output compare modules to generate the required baud clock signal when the UART is receiving data or in an Idle state.

Affected Silicon Revisions

A3	A4	A5					
X	X	X					

3. Module: UART

When the UART is in 4x mode (BRGH = 1) and using two Stop bits (STSEL = 1), it may sample the first Stop bit instead of the second one.

This issue does not affect the other UART configurations.

Work around

Use the 16x baud rate option (BRGH = 0) and adjust the baud rate accordingly.

Affected Silicon Revisions

A3	A4	A5					
X	X	X					

4. Module: UART

The UART error interrupt may not occur, or may occur at an incorrect time, if multiple errors occur during a short period of time.

Work around

Read the error flags in the UxSTA register whenever a byte is received to verify the error status. In most cases, these bits will be correct, even if the UART error interrupt fails to occur.

Affected Silicon Revisions

A3	A4	A5					
X	X	X					

5. Module: I²C™

If there are two I²C devices on the bus, one of them is acting as the Master receiver and the other as the Slave transmitter. If both devices are configured for 10-bit addressing mode, and have the same value in the A10 and A9 bits of their addresses, then when the Slave select address is sent from the Master, both the Master and Slave acknowledge it. When the Master sends out the read operation, both the Master and the Slave enter into Read mode and both of them transmit the data. The resultant data will be the ANDing of the two transmissions.

Work around

In all I²C devices, the addresses as well as bits A10 and A9 should be different.

Affected Silicon Revisions

A3	A4	A5					
X	X	X					

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6. Module: I²C

When the I²C module is operating in either Master or Slave mode, after the ACKSTAT bit is set when receiving a NACK, it may be cleared by the reception of a Start or Stop bit.

Work around

Store the value of the ACKSTAT bit immediately after receiving a NACK.

Affected Silicon Revisions

A3	A4	A5					
X	X	X					

7. Module: I²C

In 10-bit Addressing mode, some address matches do not set the RBF flag or load the receive register I2CxRCV if the lower address byte matches the reserved addresses. In particular, these include all addresses with the form XX0000XXXX and XX1111XXXX, with the following exceptions:

- 001111000X
- 011111001X
- 101111010X
- 111111011X

Work around

Ensure that the lower address byte in 10-bit Addressing mode does not match any 7-bit reserved addresses.

Affected Silicon Revisions

A3	A4	A5					
X	X	X					

8. Module: I²C

When the I²C module is configured as a 10-bit slave with an address of 0x102, the I2CxRCV register content for the lower address byte is 0x01 rather than 0x02; however, the module acknowledges both address bytes.

Work around

None.

Affected Silicon Revisions

A3	A4	A5					
X	X	X					

9. Module: SPI

In framed SPI mode, when the FRMDLY bit (SPIxCON2<1>) is cleared and the SMP bit (SPIxCON1<9>) is cleared, frame sync pulses do not get generated.

Work around

None.

Affected Silicon Revisions

A3	A4	A5					
X	X	X					

10. Module: Internal Voltage Regulator

When the VREGS bit (RCON<8>) is set to a logic '0', the device may Reset and a higher sleep current may be observed.

Work around

Ensure the VREGS bit (RCON<8>) is set to a logic '1' for device Sleep mode operation.

Affected Silicon Revisions

A3	A4	A5					
X	X	X					

11. Module: PSV Operations

An address error trap occurs in certain addressing modes when accessing the first four bytes of an PSV page. This only occurs when using the following addressing modes:

- MOV.D
- Register Indirect Addressing (word or byte mode) with pre/post-decrement

Work around

Do not perform PSV accesses to any of the first four bytes using the above addressing modes. For applications using the C language, MPLAB C30 version 3.11 or higher, provides the following command-line switch that implements a work around for the erratum.

```
-merrata=psv_trap
```

Refer to the `readme.txt` file in the MPLAB C30 v3.11 tool suite for further details.

Affected Silicon Revisions

A3	A4	A5					
X	X	X					

12. Module: CPU

The EXCH instruction does not execute correctly.

Work around

If writing source code in assembly, the recommended work around is to replace:

```
EXCH Wsource, Wdestination
```

with:

```
PUSH Wdestination
MOV Wsource, Wdestination
POP Wsource
```

If using the MPLAB C30 C compiler, specify the compiler option: `-merrata=exch` (*Project > Build Options > Projects > MPLAB C30 > Use Alternate Settings*).

Affected Silicon Revisions

A3	A4	A5					
X	X	X					

13. Module: SPI

Writing to the SPIxBUF register as soon as the TBF bit is cleared will cause the SPI module to ignore the written data. Applications which use SPI with DMA will not be affected by this erratum.

Work around

After the TBF bit is cleared, wait for a minimum duration of one SPI Clock before writing to the SPIxBUF register.

Alternatively, do one of the following:

- Poll the RBF bit and wait for it to get set before writing to the SPIxBUF register
- Poll the SPI Interrupt flag and wait for it to get set before writing to the SPIxBUF register
- Use an SPI Interrupt Service Routine
- Use DMA

Affected Silicon Revisions

A3	A4	A5					
X	X	X					

14. Module: ECAN

ECAN module may not transmit Buffer 0 data if Buffer 1 data is queued first for the transmission. This problem is specific to transmit Buffers 0 and 1 only.

Work around

The issue can be fixed by setting reserved bit 11 in CiCTRL1 register to 1. Note that the module reset value for this bit is zero.

Affected Silicon Revisions

A3	A4	A5					
X	X	X					

15. Module: UART

The UART module will not generate consecutive break characters. Trying to perform a back-to-back Break character transmission will cause the UART module to transmit the dummy character used to generate the first Break character instead of transmitting the second Break character. Break characters are generated correctly if they are followed by non-Break character transmission.

Work around

None.

Affected Silicon Revisions

A3	A4	A5					
X	X	X					

16. Module: QEI

When the TQCS and TQGATE bits in the QEIxCON register are set, a QEI interrupt should be generated after an input pulse on the QEA input. This interrupt is not generated in the affected silicon.

Work around

None.

Affected Silicon Revisions

A3	A4	A5					
X	X	X					

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17. Module: QEI

When the TQCS and TQGATE bits in the QEIxCON register are set, the POSCNT counter should not increment but erroneously does, and if allowed to increment to match MAXCNT, a QEI interrupt will be generated.

Work around

To prevent the erroneous increment of POSCNT while running the QEI in Timer Gated Accumulation mode, initialize MAXCNT = 0.

Affected Silicon Revisions

A3	A4	A5					
X	X	X					

18. Module: I/O

While device is being programmed via PGECx/ PGEDx pin pair, device pin with SDO1 functionality may start toggling.

Work around

None.

Affected Silicon Revisions

A3	A4	A5					
X	X	X					

19. Module: ADC

If the ADC module is in an enabled state when the device enters Sleep mode as a result of executing a PWRSAV #0 instruction, the device power-down current (IPD) may exceed the specifications listed in the device data sheet. This may happen even if the ADC module is disabled by clearing the ADON bit prior to entering Sleep mode.

Work arounds

Work around 1:

In order to remain within the IPD specifications listed in the device data sheet, the user software must completely disable the ADC module by setting the ADC Module Disable bit in the corresponding Peripheral Module Disable register (PMDx), prior to executing a PWRSAV #0 instruction.

Note: The ADC module must be reinitialized by the user application before resuming ADC operation.

Work around 2:

If the ADC module was previously initialized and enabled, before entering Sleep, execute the lines of code provided in Example 1.

Note: Unlike **Work around 1**, the user application does not need to reinitialize the ADC module; however, it is necessary to re-enable the ADC module by setting the ADON bit after waking from Sleep.

Affected Silicon Revisions

A3	A4	A5					
X	X	X					

EXAMPLE 1:

```
AD1CON1bits.ADON = 0;              //Disable the ADC module
__asm__ volatile ("REPEAT #50");   //Wait 50 TCY
__asm__ volatile ("NOP");          //Repeat NOP 51 times
Sleep();                           // Execute PWRSAV #0 and go to Sleep
```

20. Module: All

The affected silicon revisions listed below are not warranted for operation at 150ºC.

Work around

Only use the affected revisions of silicon for Hi-Temp operating range from -40ºC to +140ºC.

Affected Silicon Revisions

A3	A4	A5					
X	X						

21. Module: Sleep Mode

The device power-down current (IPD) exceeds the specifications listed in the device data sheet. The actual power-down current specifications are shown in Table 3.

The IPD values in Table 3 were measured with all peripherals and clocks shut down, with the exception of the ADC module(s).

The following ADC settings were enabled for each ADC module prior to executing the `PWRSAV` instruction:

- ADON = `1`
- VCFG = `1`
- AD12B = `1`
- ADxMD = `0`

All I/Os were configured as inputs and pulled to VSS. Peripherals such as the Watchdog Timer, etc., were switched off.

Work around

None.

Affected Silicon Revisions

A3	A4	A5					
X	X						

TABLE 3: DC CHARACTERISTICS: POWER-DOWN CURRENT (IPD)

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended			
Parameter No.	**Typical**	**Max**	**Units**	**Conditions**		
Power-Down Current (IPD)						
DC60d	400	500	µA	-40°C	3.3V	Base Power-Down Current
DC60a	400	500	µA	+25°C		
DC60b	500	800	µA	+85°C		
DC60c	1000	1500	µA	+125°C		

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22. Module: CPU

When a previous `DISI` instruction is active (i.e., the DISICNT register is non-zero), and the value of the DISICNT register is updated manually, the DISICNT register freezes and disables interrupts permanently.

Work around

Avoid updating the DISICNT register manually. Instead, use the `DISI #n` instruction with the required value for '`n`'.

Affected Silicon Revisions

A3	A4	A5					
X	X	X					

23. Module: CPU

When using the Signed 32-by-16-bit Division instruction, `div.sd`, the overflow bit does not always get set when an overflow occurs.

Work around

Test for and handle overflow conditions outside of the `div.sd` instruction.

Affected Silicon Revisions

A3	A4	A5					
X	X	X					

24. Module: UART

When using UTXISEL = `01` (Interrupt when last character is shifted out of the Transmit Shift Register) and the final character is being shifted out through the Transmit Shift Register, the Transmit (TX) Interrupt may occur before the final bit is shifted out.

Work around

If it is critical that the interrupt processing occur only when all transmit operations are complete. Hold off the interrupt routine processing by adding a loop at the beginning of the routine that polls the Transmit Shift Register Empty bit (TRMT) before processing the rest of the interrupt.

Affected Silicon Revisions

A3	A4	A5					
X	X	X					

25. Module: JTAG

JTAG Flash programming is not supported.

Work around

None.

Affected Silicon Revisions

A3	A4	A5					
X	X	X					

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS70594**C**):

Note:	Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

No issues to report at this time.

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APPENDIX A: REVISION HISTORY

Rev A Document (5/2009)

Initial release of this document; issued for revision A3 and A4 silicon.

Includes silicon issues 1 (ECAN™), 2-4 (UART), 5-8 (I^2C™), 9 (SPI), 10 (Internal Voltage Regulator), 11 (PSV Operations), 12 (CPU), 13 (SPI) and 14 (ECAN).

Rev B Document (8/2009)

Added silicon issues 15 (UART), 16-17 (QEI) and 18 (I/O).

Rev C Document (6/2010)

Updated silicon issue 12 (CPU).

Added silicon issue 19 (ADC) and data sheet clarification 1 (DC Characteristics: I/O Pin Input Specifications).

Rev D Document (10/2010)

Updated the work around in silicon issue 19 (ADC).

Added silicon issue 20 (All).

Rev E Document (3/2011)

Revised silicon revision to A5 and removed data sheet clarification 1.

Added silicon issue 21 (Sleep Mode).

Rev F Document (4/2011)

Updated the affected revisions for silicon issue 19 (ADC).

Rev G Document (11/2011)

Added silicon issues 22 (CPU), 23 (CPU), 24 (UART), and 25 (JTAG).

NOTES:

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ISBN: 978-1-61341-816-1

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08/02/11

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