



SC8673040L

Asymmetric Dual Silicon N-ch Power MOS FET

For DC-DC Converter

■ Features

- Low Drain-source On-state Resistance : RDS(on) typ.
FET1 : 10 mΩ (VGS = 4.5 V), FET2 : 1.9 mΩ (VGS = 4.5 V)
- Halogen-free / RoHS compliant
(EU RoHS / UL-94 V-0 / MSL : Level 1 compliant)

■ Marking Symbol : A2

■ Packaging

Embossed type (Thermo-compression sealing) : 3 000 pcs / reel (standard)

■ Absolute Maximum Ratings Ta = 25 °C

Parameter	Symbol	Rating		Unit
		FET1	FET2	
Drain to Source Voltage	VDS	30	30	V
Gate to Source Voltage	VGS	±20	±20	V
Drain Current	Package limited	ID1	16	A
	DC *1	ID2	10	
Drain Current (Pulsed) *1 *2	IDp	48	138	A
Total Power Dissipation	Ta = 25 °C, DC *1	PD1	1.7	W
	Ta = 25 °C, DC *3	PD2	1	
	Tc = 25 °C	PD3	19	
Thermal Resistance	Channel to Ambient *1	Rth(ch-a)1	70	°C / W
	Channel to Ambient *3	Rth(ch-a)2	125	
	Channel to Case	Rth(ch-c)	6.6	
Channel Temperature	Tch	150		°C
Operating ambient temperature	Topr	-40 to +85		
Storage Temperature Range	Tstg	-55 to +150		
Avalanche Current (Single pulse) *4	IAR	8	23	A
Avalanche Energy (Single pulse) *4	EAR	8	61	mJ

Note *1 Device mounted on a glass-epoxy board in Figure 1.1 and 1.2

*2 Pulse test : Ensure that the channel temperature does not exceed 150 °C

*3 Device mounted on a glass-epoxy board in Figure 1.3

*4 VDD = 24 V, VGS = 10 to 0 V, L = 0.1 mH, Tch = 25 °C (initial)

Outline and Figures

FR4 Glass-Epoxy Board (25.4 mm × 25.4 mm × 0.8 mm)

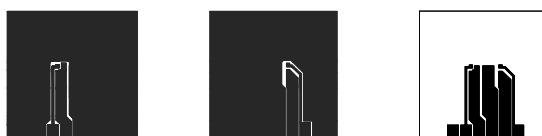
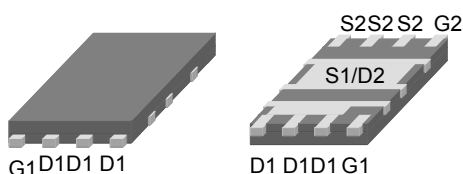
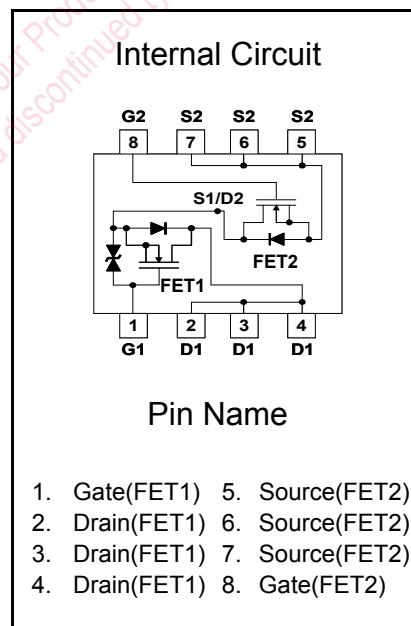
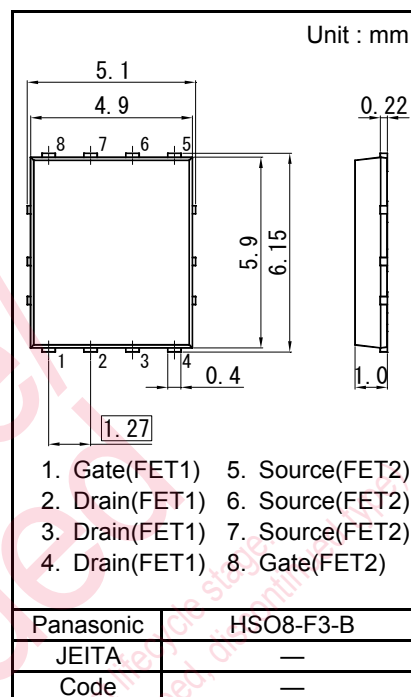


Figure 1.1 (FET1) Figure 1.2 (FET2) Figure 1.3 (FET1, FET2)





■ Electrical Characteristics Ta = 25 °C ± 3 °C

FET1

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Drain-source Breakdown Voltage	VDSS	ID = 1 mA, VGS = 0 V	30			V
Zero Gate Voltage Drain Current	IDSS	VDS = 30 V, VGS = 0 V			10	μA
Gate-source Leakage Current	IGSS	VGS = ±16 V, VDS = 0 V			±10	μA
Gate-source Threshold Voltage	Vth	ID = 1.01 mA, VDS = 10 V	1		3	V
Drain-source On-state Resistance	RDS(on)1	ID = 8 A, VGS = 10 V		7	10	mΩ
	RDS(on)2	ID = 8 A, VGS = 4.5 V		10	14	
Input Capacitance	Ciss	VDS = 10 V, VGS = 0 V f = 1 MHz		780	1 092	pF
Output Capacitance	Coss			160	224	
Reverse Transfer Capacitance	Crss			61	98	
Turn-on Delay Time ^{*1}	td(on)	VDD = 15 V, VGS = 0 to 10 V		7		ns
Rise Time ^{*1}	tr	ID = 8 A		3		
Turn-off Delay Time ^{*1}	td(off)	VDD = 15 V, VGS = 10 to 0 V		34		ns
Fall Time ^{*1}	tf	ID = 8 A		4		
Total Gate Charge	Qg	VDD = 15 V, VGS = 0 to 4.5 V ID = 8 A		6.3		nC
Gate to Source Charge	Qgs			2.5		
Gate to Drain Charge	Qgd			2.1		
Gate resistance	rg	f = 5 MHz		1.2	3	Ω

Body Diode Characteristic

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Diode Forward Voltage	VSD	IS = 8 A, VGS = 0 V		0.8	1.2	V

Note : 1. Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 Measuring methods for transistors.

2. *1 Measurement circuit for Turn-on Delay Time / Rise Time / Turn-off Delay Time / Fall Time

FET2

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Drain-source Breakdown Voltage	VDSS	ID = 1 mA, VGS = 0 V	30			V
Zero Gate Voltage Drain Current	IDSS	VDS = 30 V, VGS = 0 V			10	μA
Gate-source Leakage Current	IGSS	VGS = ±16 V, VDS = 0 V			±10	μA
Gate-source Threshold Voltage	Vth	ID = 5.85 mA, VDS = 10 V	1.3		3	V
Drain-source On-state Resistance	RDS(on)1	ID = 23 A, VGS = 10 V		1.6	2.2	mΩ
	RDS(on)2	ID = 23 A, VGS = 4.5 V		1.9	2.5	
Input Capacitance	Ciss	VDS = 10 V, VGS = 0 V f = 1 MHz		4 900	6 860	pF
Output Capacitance	Coss			570	798	
Reverse Transfer Capacitance	Crss			410	656	
Turn-on Delay Time ^{*1}	td(on)	VDD = 15 V, VGS = 0 to 10 V		18		ns
Rise Time ^{*1}	tr	ID = 23 A		14		
Turn-off Delay Time ^{*1}	td(off)	VDD = 15 V, VGS = 10 to 0 V		75		ns
Fall Time ^{*1}	tf	ID = 23 A		11		
Total Gate Charge	Qg	VDD = 15 V, VGS = 0 to 4.5 V ID = 23 A		37		nC
Gate to Source Charge	Qgs			12		
Gate to Drain Charge	Qgd			14		
Gate resistance	rg	f = 5 MHz		1.2	3	Ω

Body Diode Characteristic

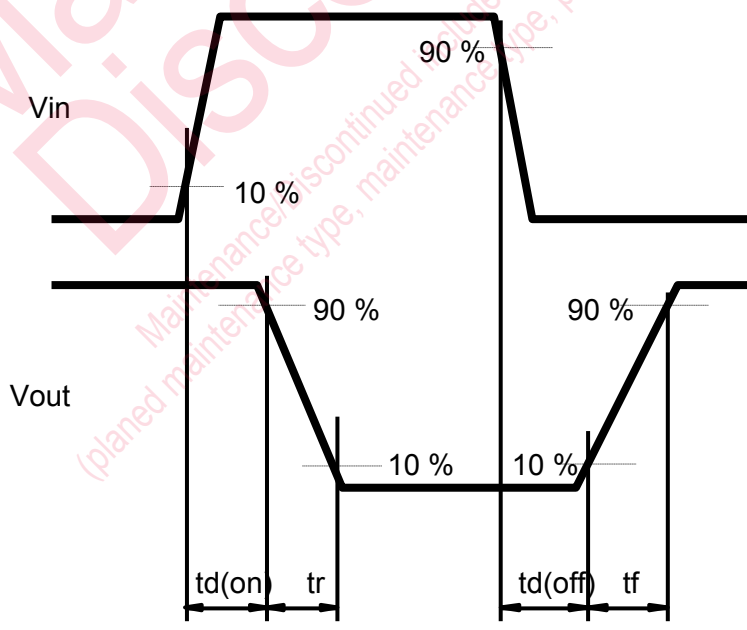
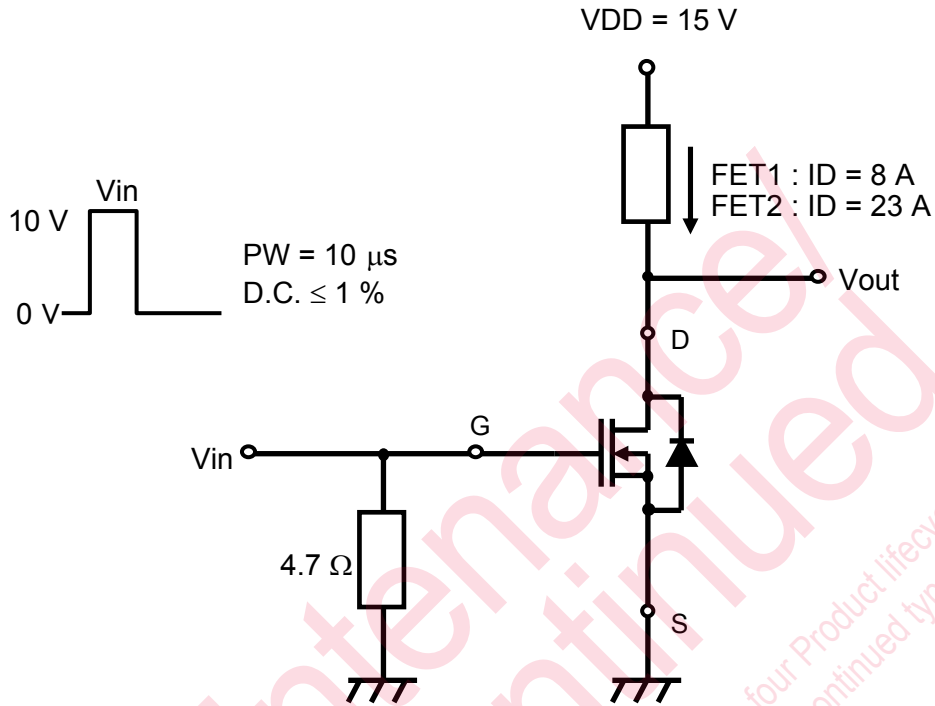
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Diode Forward Voltage	VSD	IS = 23 A, VGS = 0 V		0.8	1.2	V

Note : 1. Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 Measuring methods for transistors.

2. *1 Measurement circuit for Turn-on Delay Time / Rise Time / Turn-off Delay Time / Fall Time



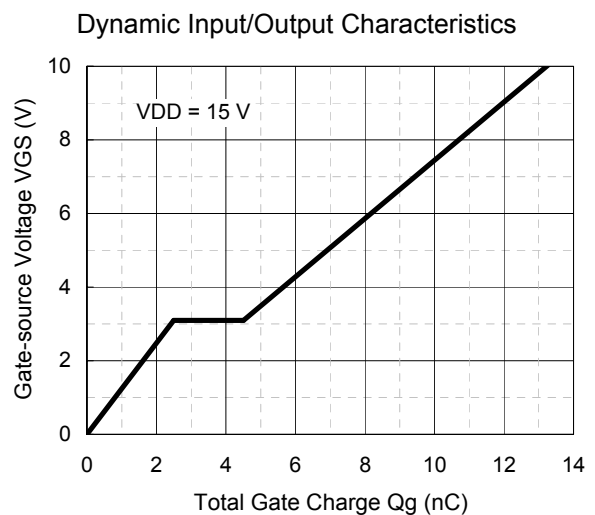
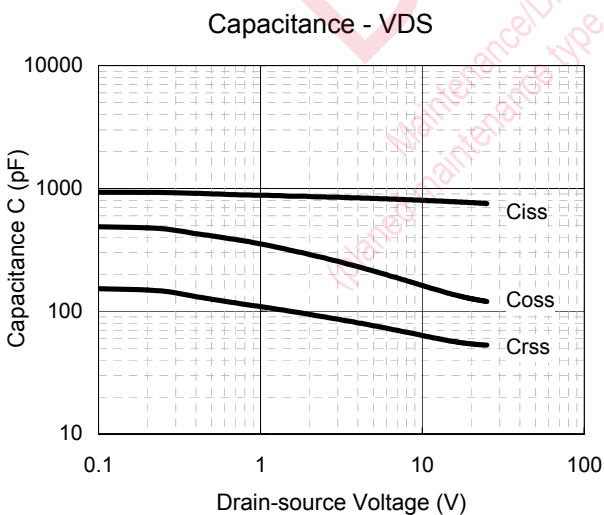
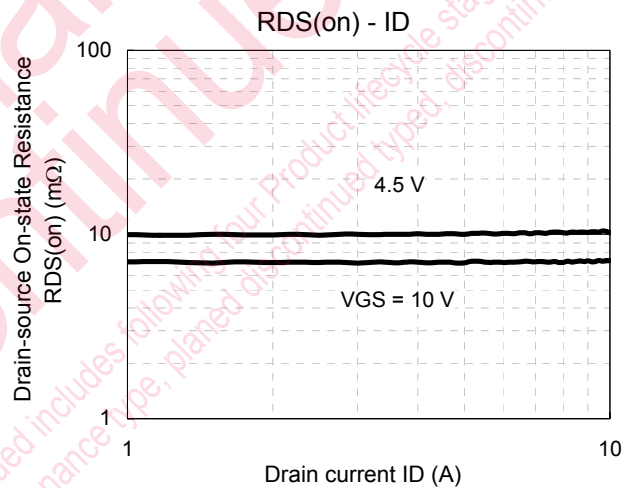
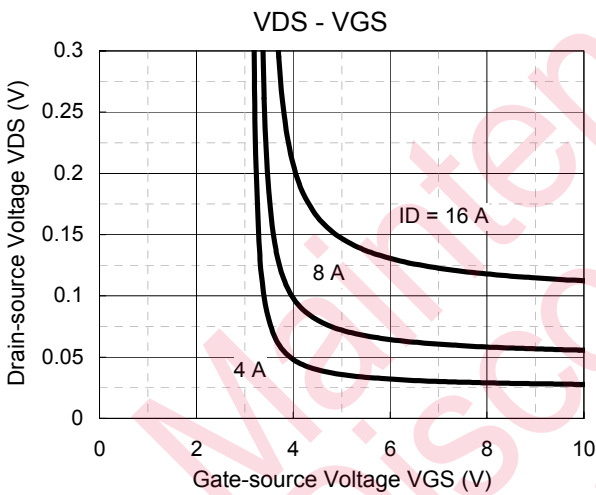
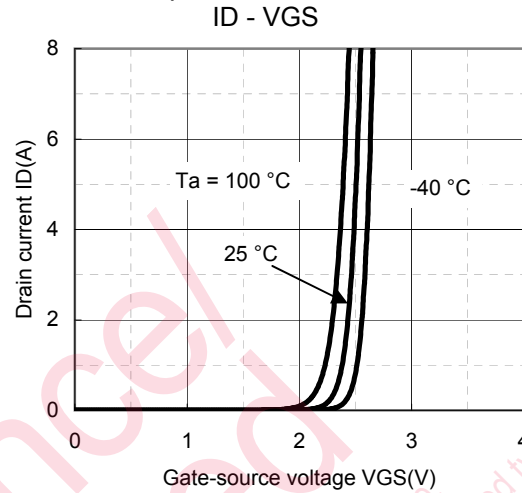
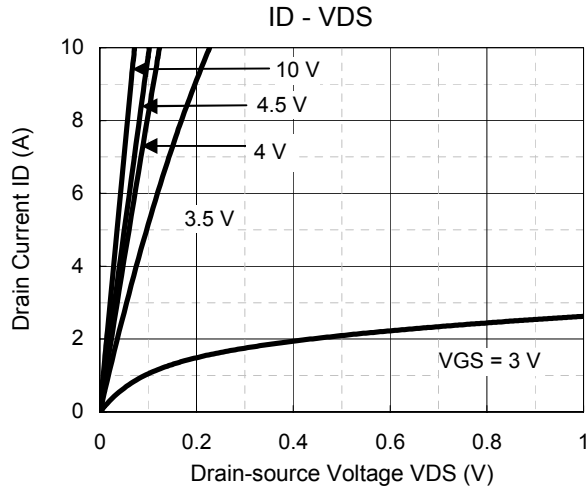
*1 Measurement circuit for Turn-on Delay Time / Rise Time / Turn-off Delay Time / Fall Time





FET1

Technical Data (reference)

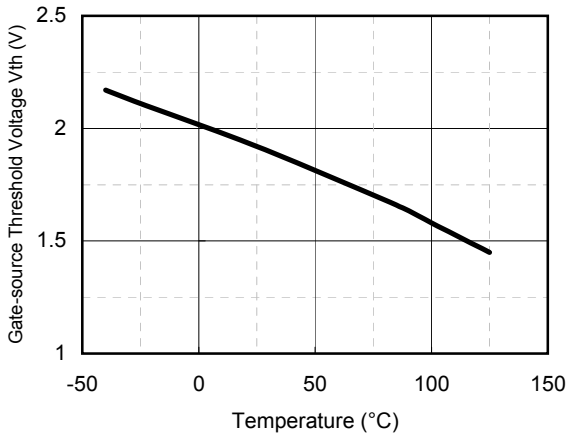




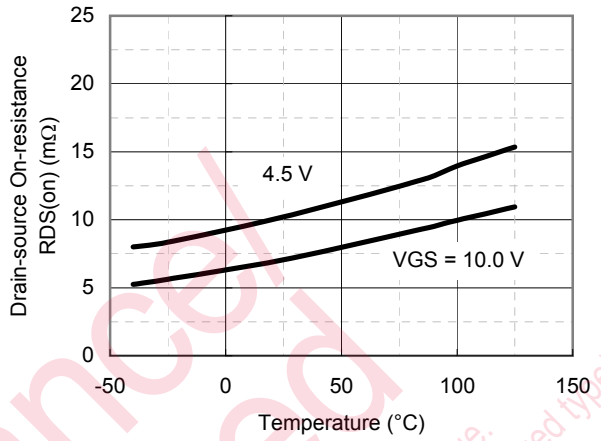
FET1

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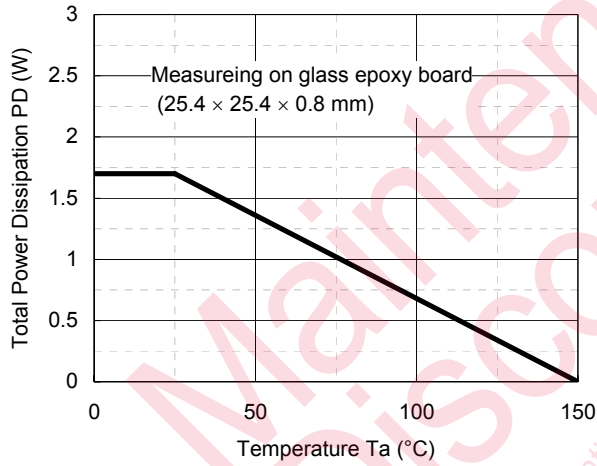
V_{th} - T_a



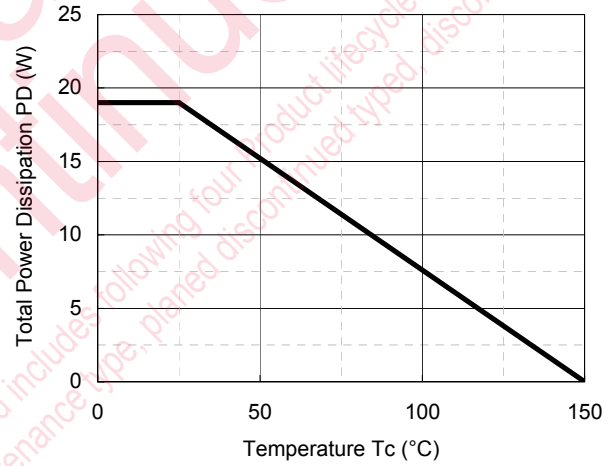
RDS(on) - T_a



PD - T_a



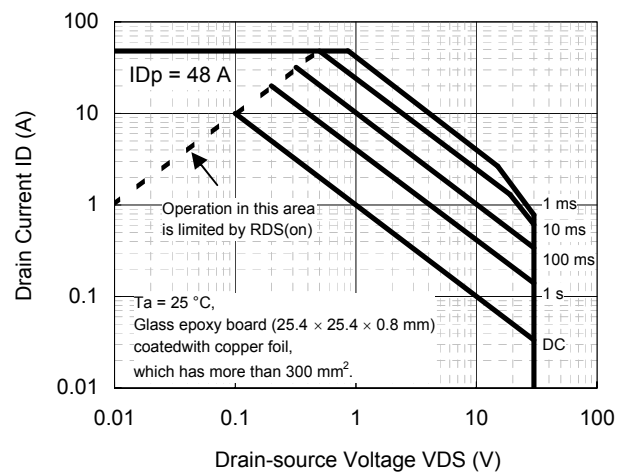
PD - T_c



R_{th} - t_{sw}



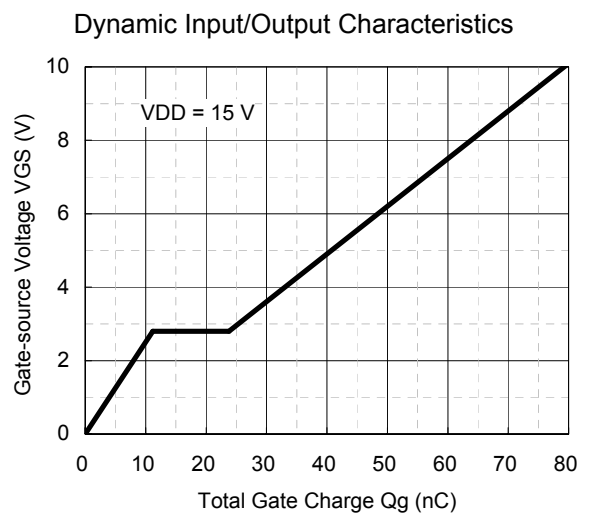
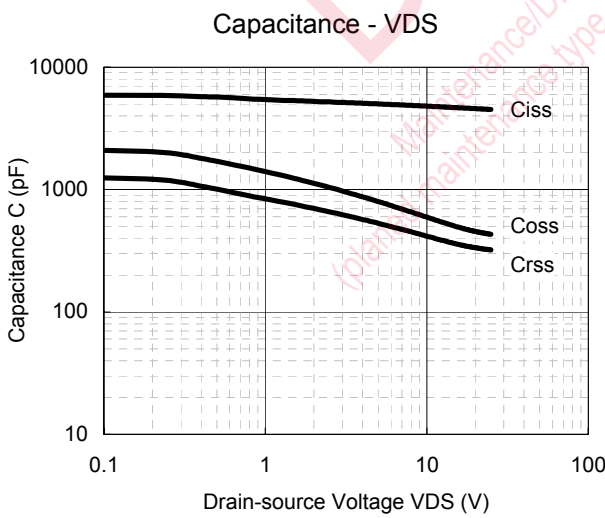
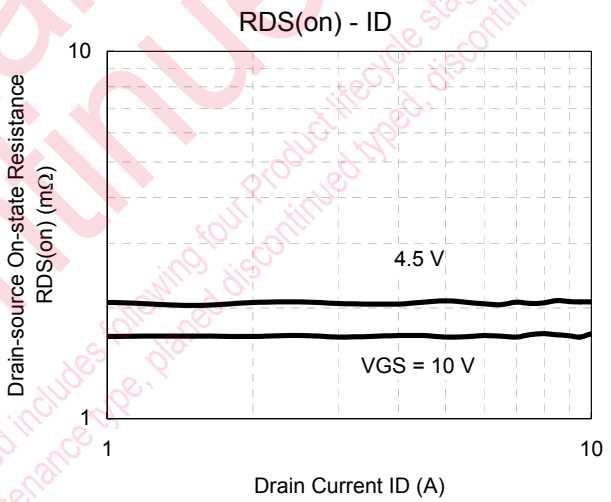
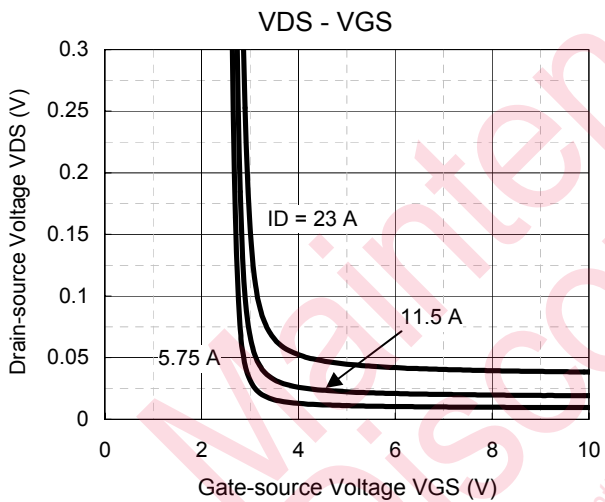
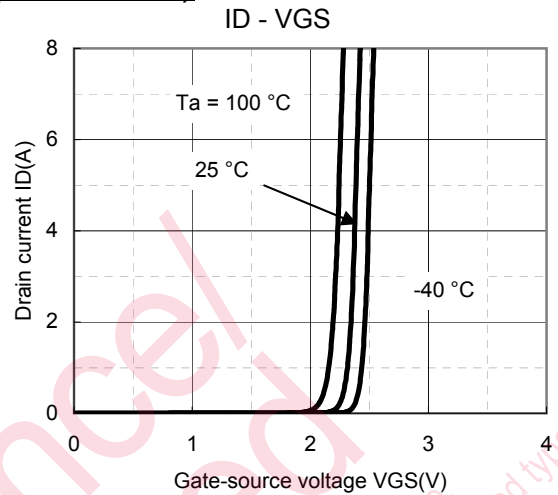
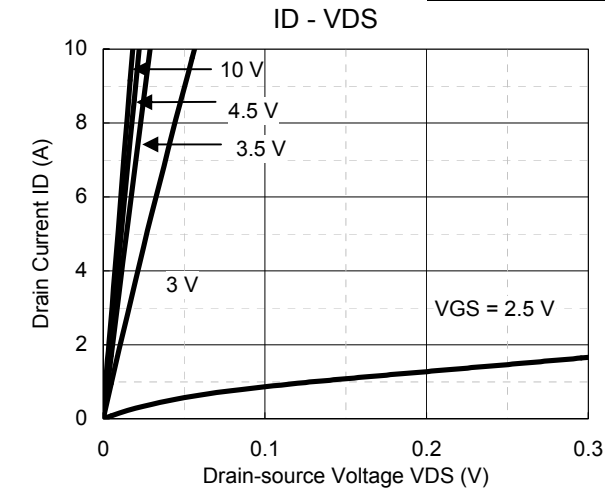
Safe Operating Area





FET2

Technical Data (reference)

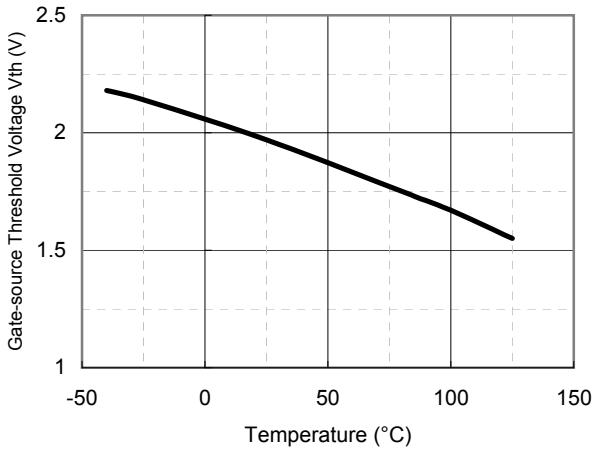




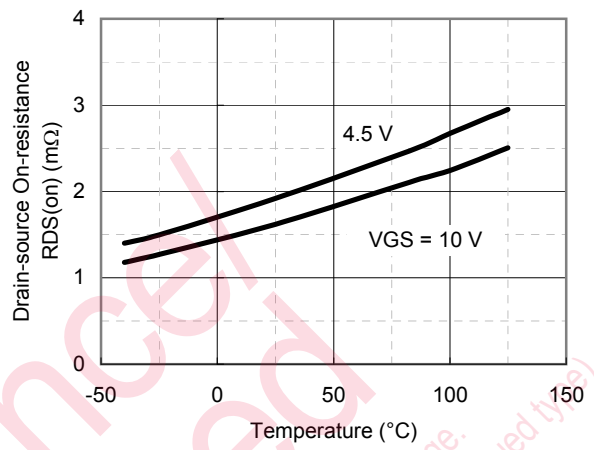
FET2

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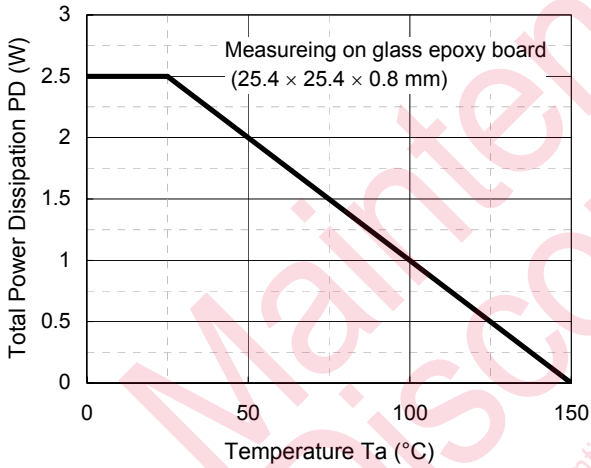
V_{th} - T_a



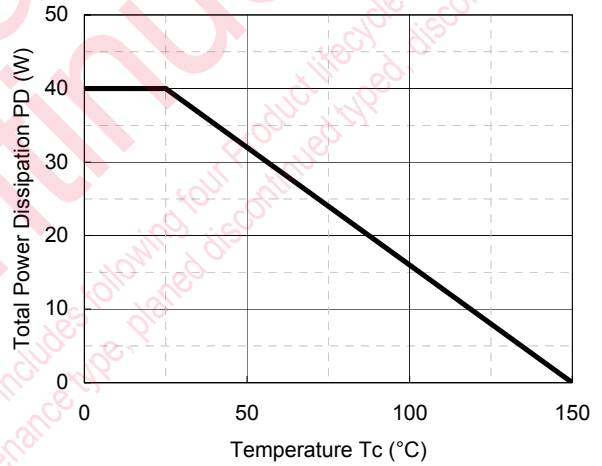
R_{DS(on)} - T_a



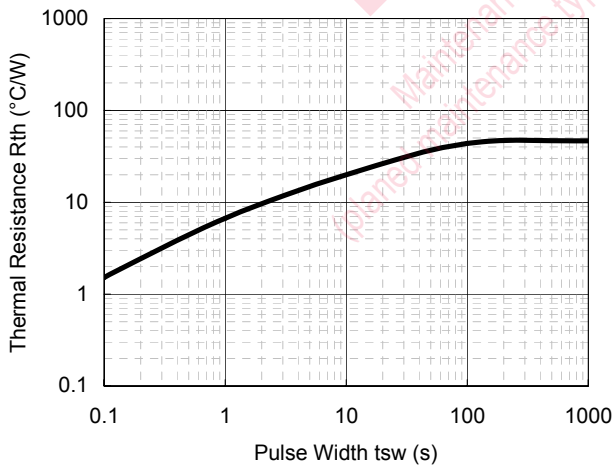
PD - T_a



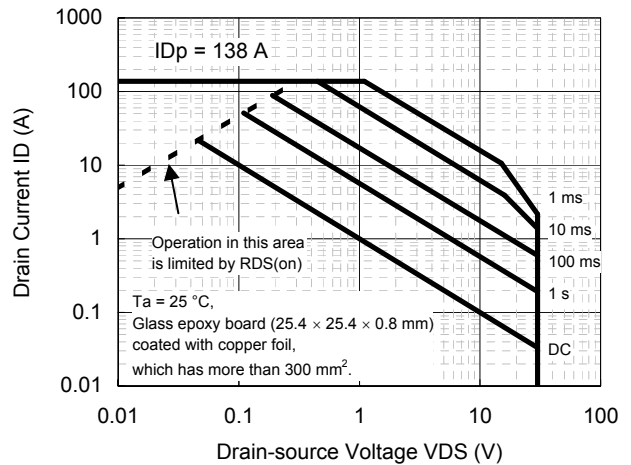
PD - T_c



R_{th} - t_{sw}



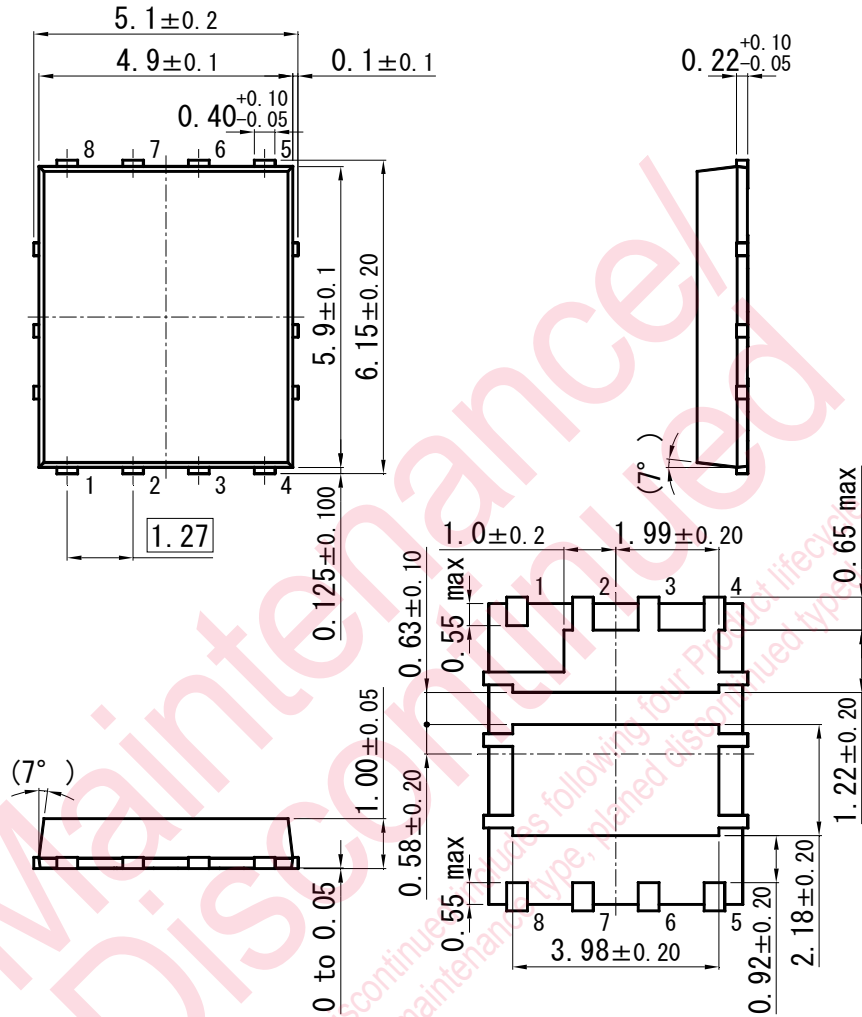
Safe Operating Area



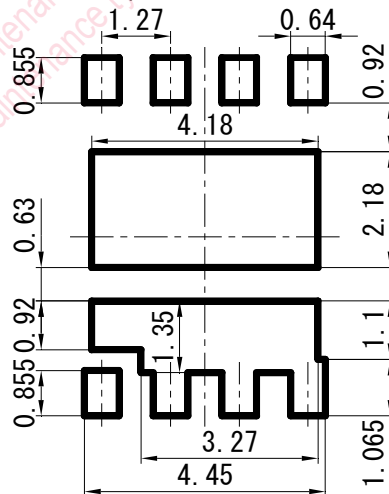


HSO8-F3-B

Unit : mm



■ Land Pattern (Reference) (Unit : mm)



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