VR11.1, VR12 Compatible Synchronous Rectified Buck MOSFET Driver

ISL6627

The ISL6627 is a high frequency MOSFET driver designed to drive upper and lower power N-Channel MOSFETs in a synchronous rectified buck converter topology. The advanced PWM protocol of ISL6627 is specifically designed to work with Intersil VR11.1, VR12 controllers and combined with N-Channel MOSFETs to form a complete core-voltage regulator solution for advanced microprocessors. When ISL6627 detects a $\overline{\text{PSI}}$ protocol sent by an Intersil VR11.1, VR12 controller, it activates Diode Emulation (DE) operation; otherwise, it operates in normal Continuous Conduction Mode (CCM) PWM mode.

To further enhance light load efficiency, the ISL6627 enables diode emulation operation during $\overline{\text{PSI}}$ mode. This allows Discontinuous Conduction Mode (DCM) by detecting when the inductor current reaches zero and subsequently turning off the low side MOSFET to prevent it from sinking current.

When ISL6627 detects Diode Braking command from the PWM, it turns off both gates and reduces overshoot in load transient situations.

An advanced adaptive shoot-through protection is integrated to prevent both the upper and lower MOSFETs from conducting simultaneously and to minimize dead time. The user also has the option to program the driver working in fixed propagation delay mode to optimize the regulator efficiency. The ISL6627 has a 20kΩ integrated high-side gate-to-source resistor to prevent self turn-on due to high input bus dV/dt.

Related Literature

- Technical Brief TB363 “Guidelines for Handling and Processing Moisture Sensitive Surface Mount Devices (SMDs)”
- Technical Brief TB417 “Designing Stable Compensation Networks for Single Phase Voltage Mode Buck Regulators”

Features

- Intersil VR11.1 and VR12 Compatible
- Dual MOSFET Driver for Synchronous Rectified Bridge
- Advanced Adaptive Zero Shoot-through Protection
- Programmable Fixed Deadtime for Efficiency Optimization
- Low Standby Bias Current
- 36V Internal Bootstrap Diode
- Bootstrap Capacitor Overcharge Prevention
- Supports High Switching Frequency
  - 4A Sinking Current Capability
  - Fast Rise/Fall Times and Low Propagation Delays
- Integrated High-Side Gate-to-Source Resistor to Prevent Self Turn-on Due to High Input Bus dV/dt
- Power Rails Undervoltage Protection
- Expandable Bottom Copper Pad for Enhanced Heat Sinking
- Dual Flat 10 Ld (3x3 DFN) Package
  - Near Chip-Scale Package Footprint; Improves PCB Efficiency and Thinner in Profile
- Pb-Free (RoHS Compliant)

Applications

- High Light Load Efficiency Voltage Regulators
- Core Regulators for Advanced Microprocessors
- High Current DC/DC Converters
- High Frequency and High Efficiency VRM and VRD

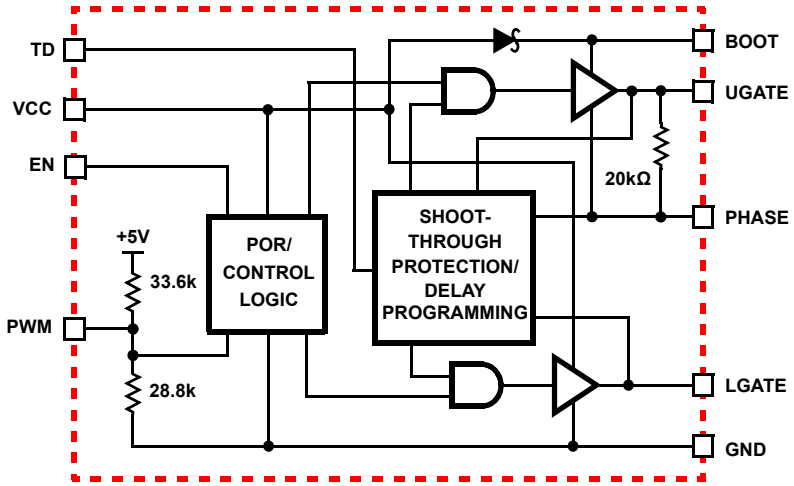
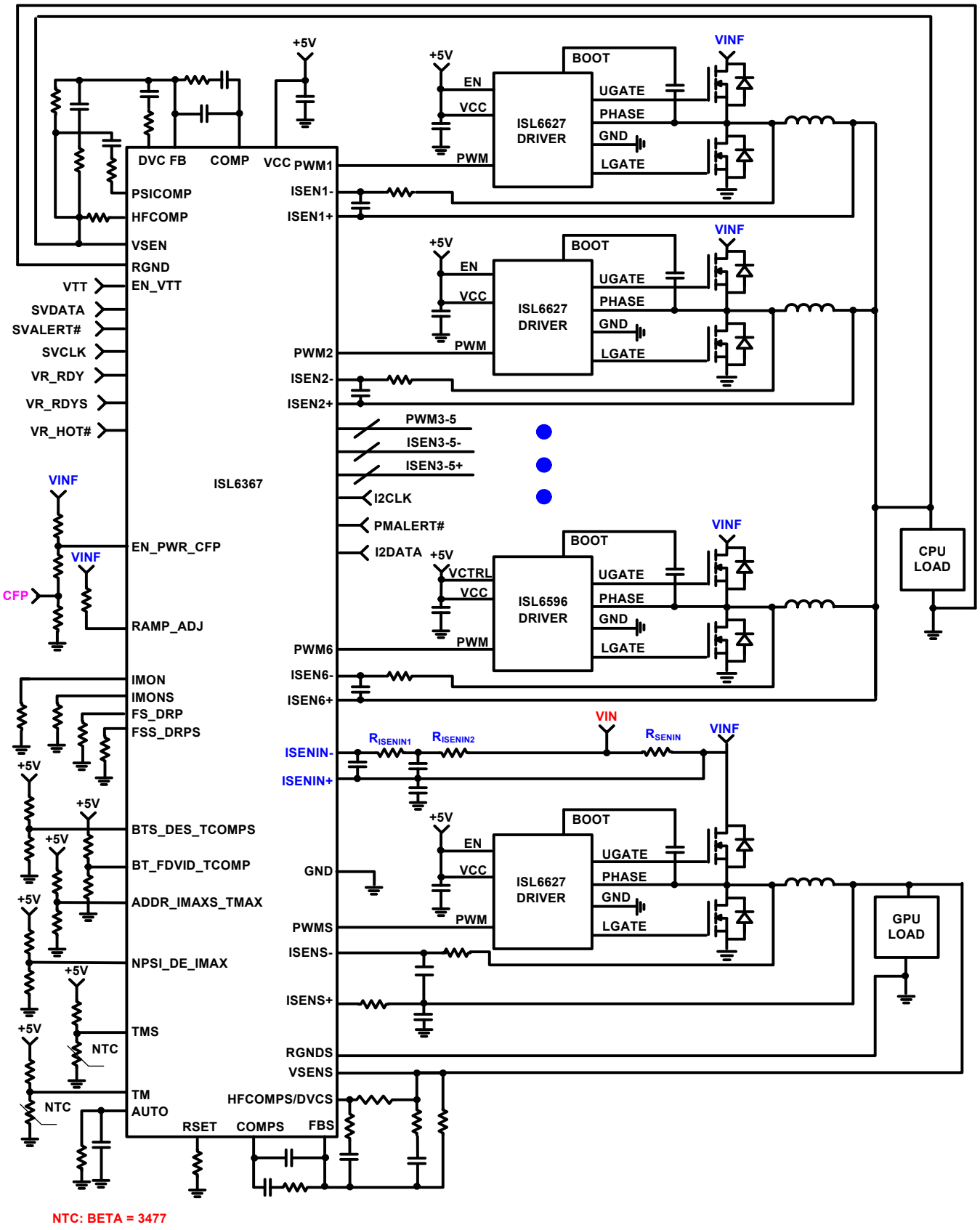


FIGURE 1. ISL6627 BLOCK DIAGRAM

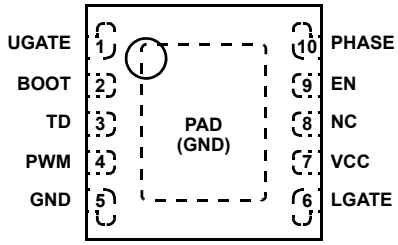
Typical Application Circuit



NTC: BETA = 3477

Pin Configuration

ISL6627
(10 LD 3x3 DFN)
TOP VIEW



Functional Pin Descriptions

PIN #	SYMBOL	DESCRIPTION
1	UGATE	Upper gate drive output. Connect to gate of high-side power N-Channel MOSFET.
2	BOOT	Floating bootstrap supply pin for the upper gate drive. Connect the bootstrap capacitor between this pin and the PHASE pin. The bootstrap capacitor provides the charge to turn on the upper MOSFET. See “Internal Bootstrap Device” on page 7 for guidance in choosing the capacitor value.
3	TD	Deadtime programming pin. Connect to ground or VCC via resistor to program fixed time delay from LGATE fall to UGATE rise or UGATE fall to LGATE rise. Open pin sets the adaptive mode. See Table 1 for more details.
4	PWM	Control input for the driver. The PWM signal can enter three distinct states during operation; see “Advanced PWM Protocol (Patent Pending)” on page 6 for further details. Connect this pin to the PWM output of the controller.
5	GND	Bias and reference ground. All signals are referenced to this node. It is also the power ground return of the driver.
6	LGATE	Lower gate drive output. Connect to gate of the low-side power N-Channel MOSFET.
7	VCC	Connect to 5V bias supply. This pin supplies power to the gate drives and small-signal circuitry. Place a high quality low ESR ceramic capacitor from this pin to GND.
8	NC	No connection.
9	EN	Enable input pin. Connect this pin high to enable the driver and low to disable the driver.
10	PHASE	Connect this pin to the SOURCE of the upper MOSFET and the DRAIN of the lower MOSFET. This pin provides a return path for the upper gate drive.
-	PAD	EPAD at ground potential. Soldering it directly to GND plane is required for thermal considerations.

Ordering Information

PART NUMBER (Notes 1, 2, 3)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
ISL6627CRZ	6627	0 to +70	10 Ld 3x3 DFN	L10.3X3
ISL6627IRZ	627I	-40 to +85	10 Ld 3x3 DFN	L10.3X3

NOTES:

1. Add “-T*” suffix for tape and reel. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL6627. For more information on MSL please see techbrief TB363.

Absolute Maximum Ratings

Supply Voltage (VCC) . . . . . -0.3V to 7V
Input Voltage (V_{EN}, V_{PWM}) . . . . . -0.3V to VCC + 0.3V
BOOT Voltage ($V_{BOOT-GND}$) . . . . . -0.3V to 25V (DC) or 36V (<200ns)
BOOT to PHASE Voltage ($V_{BOOT-PHASE}$) . . . . . -0.3V to 7V (DC)
. . . . . -0.3V to 9V (<10ns)
PHASE Voltage . . . . . GND - 0.3V to 25V (DC)
. . . . . GND -8V (<20ns Pulse Width, 10µJ) to 30V (<100ns)
UGATE Voltage. . . . . V_{PHASE} - 0.3V (DC) to V_{BOOT}
. . . . . V_{PHASE} - 5V (<20ns Pulse Width, 10µJ) to V_{BOOT}
LGATE Voltage . . . . . GND - 0.3V (DC) to VCC + 0.3V
. . . . . GND - 2.5V (<20ns Pulse Width, 5µJ) to VCC + 0.3V
Ambient Temperature Range . . . . . -40°C to +125°C
ESD Rating
Human Body Model 2.5kV
Charged Device Model 1kV
Latch Up (Tested per JESD78C; Class II, Level A) 100mA

Thermal Information

Thermal Resistance	θ_{JA} (°C/W)	θ_{JC} (°C/W)
10 Ld 3x3 DFN Package (Notes 4, 5). . . .	51	10

Maximum Junction Temperature (Plastic Package) . . . . . +150°C
Maximum Storage Temperature Range . . . . . -65°C to +150°C
Pb-Free Reflow Profile . . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Recommended Operating Conditions

Ambient Temperature Range(ISL6627IRZ) . . . . . -40°C to +85°C
Ambient Temperature Range (ISL6627CRZ) . . . . . 0°C to +70°C
Maximum Operating Junction Temperature . . . . . +125°C
Supply Voltage, VCC . . . . . 5V ±10%

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379.
5. For θ_{JC}, the “case temp” location is the center of the exposed metal pad on the package underside.

Electrical Specifications

Recommended Operating Conditions, Unless Otherwise Noted. **Boldface limits apply over the operating temperature range.**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNITS
VCC SUPPLY CURRENT						
No Load Switching Supply Current	IVCC	f_PWM = 300kHz, VCC = 5V, EN = High		1.27		mA
Standby Supply Current	IVCC	VCC = 5V, PWM 0V to 2.5V transition, EN = High		1.85		mA
		VCC = 5V, PWM 0V to 2.5V transition, EN = Low		1.15		mA
POWER-ON RESET AND ENABLE						
VCC Rising POR Threshold			**3.20**	3.85	**4.40**	V
VCC Falling POR Threshold			**3.00**	3.52	**4.00**	V
VCC POR Hysteresis			**130**	300	**530**	mV
EN High Threshold			**1.40**	1.65	**1.90**	V
EN Low Threshold			**1.20**	1.35	**1.55**	V
PWM INPUT (See “TIMING DIAGRAM” on page 6)						
Input Current	IPWM	VPWM = 5V		155		µA
		VPWM = 0V		-133		µA
Three-State Lower Gate Falling Threshold		VCC = 5V		1.6		V
Three-State Lower Gate Rising Threshold		VCC = 5V		1.1		V
Three-State Upper Gate Rising Threshold		VCC = 5V		3.2		V
Three-state Upper Gate Falling Threshold		VCC = 5V		2.8		V
UGATE Rise Time (Note 6)	t_RU	VCC = 5V, 3nF load, 10% to 90%		8		ns
LGATE Rise Time (Note 6)	t_RL	VCC = 5V, 3nF load, 10% to 90%		8		ns
UGATE Fall Time (Note 6)	t_FU	VCC = 5V, 3nF load, 10% to 90%		8		ns
LGATE Fall Time (Note 6)	t_{FL}	VCC = 5V, 3nF load, 10% to 90%		4		ns
UGATE Turn-On Propagation Delay (Note 6)	t_{PDHU}	VCC = 5V, 3nF load, adaptive		28		ns
LGATE Turn-On Propagation Delay (Note 6)	t_{PDHL}	VCC = 5V, 3nF load, adaptive		16		ns
UGATE Turn-Off Propagation Delay (Note 6)	t_{PDLU}	VCC = 5V, 3nF load		15		ns

Electrical Specifications Recommended Operating Conditions, Unless Otherwise Noted. **Boldface limits apply over the operating temperature range. (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNITS
LGATE Turn-Off Propagation Delay (Note 6)	t_{PDLL}	VCC = 5V, 3nF load		14		ns
Minimum LGATE on Time at Diode Emulation	$t_{LG\_ON\_DM}$	VCC = 5V	**230**	330	**450**	ns
PROPAGATION DELAY PROGRAMMING						
UGATE Fall to LGATE Rise Time	t_{PDUFLR}	VCC = 5V, 3nF Load, 90% to 10%, short resistor from TD to VCC		23		ns
		VCC = 5V, 3nF Load, 90% to 10%, 100kΩ resistor from TD to VCC		18		ns
		VCC = 5V, 3nF Load, 90% to 10%, 330kΩ resistor from TD to VCC		15		ns
		VCC = 5V, 3nF Load, 90% to 10%, 910kΩ resistor from TD to VCC		7		ns
		VCC = 5V, 3nF Load, 90% to 10%, short resistor from TD to GND		18		ns
LGATE Fall to UGATE Rise Time	t_{PDLFUR}	VCC = 5V, 3nF Load, 90% to 10%, short resistor from TD to GND		40		ns
		VCC = 5V, 3nF Load, 90% to 10%, 100kΩ resistor from TD to GND		25		ns
		VCC = 5V, 3nF Load, 90% to 10%, 360kΩ resistor from TD to GND		17		ns
		VCC = 5V, 3nF Load, 90% to 10%, short resistor from TD to VCC		27		ns
OUTPUT (Note 6)						
Upper Drive Source Current	I_U_SOURCE	VCC = 5V, 3nF load		2		A
Upper Drive Source Impedance	R_U_SOURCE	20mA source current		1		Ω
Upper Drive Sink Current	I_U_SINK	VCC = 5V, 3nF load		2		A
Upper Drive Sink Impedance	R_U_SINK	20mA sink current		1		Ω
Lower Drive Source Current	I_L_SOURCE	VCC = 5V, 3nF load		2		A
Lower Drive Source Impedance	R_L_SOURCE	20mA source current		1		Ω
Lower Drive Sink Current	I_L_SINK	VCC = 5V, 3nF load		4		A
Lower Drive Sink Impedance	R_L_SINK	20mA sink current		0.4		Ω

NOTES:

6. Limits established by characterization and are not production tested.
7. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

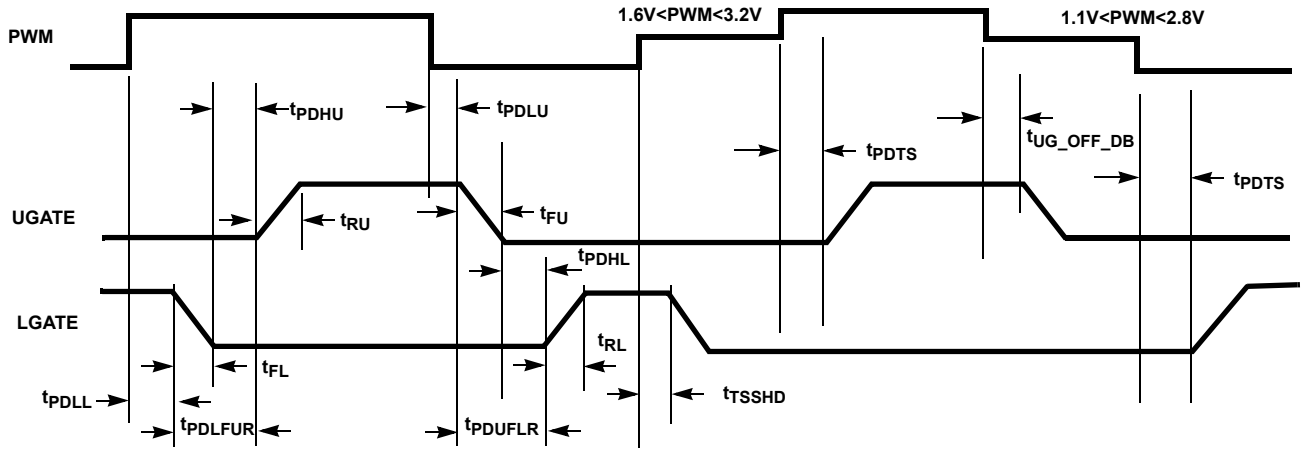


FIGURE 2. TIMING DIAGRAM

Operation and Adaptive Shoot-Through Protection

Designed for high speed switching, the ISL6627 MOSFET driver controls both high-side and low-side N-Channel FETs from one externally-provided PWM signal.

A rising transition on PWM initiates the turn-off of the lower MOSFET (see "Timing Diagram"). After a short propagation delay [t_{PDLL}], the lower gate begins to fall. Typical fall times [t_{FL}] are provided in the "*Electrical Specifications" on* page 4. Adaptive shoot-through circuitry monitors the LGATE voltage and turns on the upper gate following a short delay time [t_{PDHU}] after the LGATE voltage drops below ~1V. The user also has the option to program the propagation delay as described in "Deadtime Programming" on page 6. The upper gate drive then begins to rise [t_{RU}] and the upper MOSFET turns on.

A falling transition on PWM indicates the turn-off of the upper MOSFET and the turn-on of the lower MOSFET. A short propagation delay [t_{PDLU}] is encountered before the upper gate begins to fall [t_{FU}]. The adaptive shoot-through circuitry monitors the UGATE-PHASE voltage and turns on the lower MOSFET a short delay time [t_{PDHL}], after the upper MOSFET's gate voltage drops below 1V. The lower gate then rises [t_{RL}], turning on the lower MOSFET. These methods prevent both the lower and upper MOSFETs from conducting simultaneously (shoot-through), while adapting the dead time to the gate charge characteristics of the MOSFETs being used. The user also has the option to program the propagation delay as described in "Deadtime Programming" on page 6.

This driver is optimized for voltage regulators with a large step down ratio. The lower MOSFET is usually sized larger compared to the upper MOSFET because the lower MOSFET conducts for a longer time during a switching period. The lower gate driver is therefore sized much larger to meet this application requirement. The 0.4Ω ON-resistance and 4A sink current capability enable the lower gate driver to absorb the charge injected into the lower gate through the drain-to-gate capacitor of the lower MOSFET and help prevent shoot through caused by the self turn-on of the lower MOSFET due to high dV/dt of the switching node.

Advanced PWM Protocol (Patent Pending)

The advanced PWM protocol of ISL6627 is specifically designed to work with Intersil VR11.1 and VR12 controllers. When ISL6627 detects a PSI# protocol sent by an Intersil VR11.1/VR12 controller, it turns on diode emulation operation; otherwise, it remains in normal CCM PWM mode.

Note that for a PWM low to tri-level (2.5V) transition, the LGATE will not turn off until the its diode emulation minimum ON-time of 330ns (typically) passes.

Diode Emulation

Diode emulation allows for higher converter efficiency under light-load situations. With diode emulation active, the ISL6627 detects the zero current crossing of the output inductor and turns off LGATE, preventing the low side MOSFET from sinking current and ensuring discontinuous conduction mode (DCM) is achieved. In DCM mode, LGATE has a minimum ON-time of 330ns (typically).

Deadtime Programming

The part provides the user with the option to program either of the two gate propagation delays (as defined in Figure 3) in order to optimize the deadtime and maximize the efficiency of the circuit. Tying the TD pin to either GND or VCC through a specified-value resistor leads the driver to operate in fixed gate propagation delay mode. Leaving the TD pin floating results in the driver operating in adaptive deadtime mode. Refer to Table 1 for typical programming resistor value options. Propagation delay has a typical tolerance of 30%. As actual deadtime depends on FET switching transition characteristics, while operating in fixed propagation delay mode, the user needs to monitor the gate transitions under worst-case operating conditions and use appropriate design margin to prevent eventual shoot-through due to insufficient dead time.

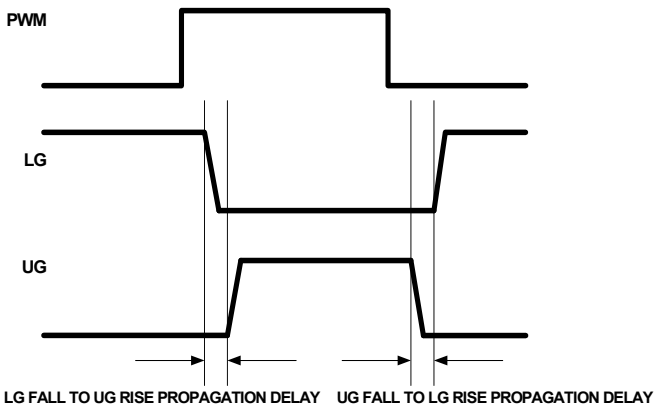


FIGURE 3. PROGRAMMABLE PROPAGATION DELAY ILLUSTRATION

TABLE 1. TYPICAL DELAY PROGRAMMING RESISTOR VALUE

RESISTOR FROM TD TO VCC (kΩ)	RESISTOR FROM TD TO GND (kΩ)	LG FALL TO UG RISE DELAY (ns)	UG FALL TO LG RISE DELAY (ns)
short	-	27	23
100	-	27	18
330	-	27	15
910	-	27	7
-	Short	40	18
-	100	25	18
-	360	17	18
Floating	Floating	Adaptive	Adaptive

Power-On Reset (POR) Function

VCC voltage level is monitored at all times. Once the VCC voltage exceeds 3.85V (typically), operation of the driver is enabled and the PWM input signal takes control of the gate drivers. If VCC drops below the falling threshold of 3.52V (typically), operation of the driver is disabled.

Internal Bootstrap Device

ISL6627 features an internal bootstrap schottky diode. Simply adding an external capacitor across the BOOT and PHASE pins completes the bootstrap circuit. The bootstrap function is also designed to prevent the bootstrap capacitor from overcharging due to the large negative swing at the trailing-edge of the PHASE node excursion. This reduces the potential for overstressing the upper driver.

The bootstrap capacitor must have a voltage rating above the maximum VCC voltage. Its capacitance value can be estimated from Equation 1:

$$C_{BOOT\_CAP} \geq \frac{Q_{GATE}}{\Delta V_{BOOT\_CAP}}$$

$$Q_{GATE} = \frac{Q_{G1} \bullet VCC}{V_{GS1}} \bullet N_{Q1} \qquad \text{(EQ. 1)}$$

where Q_{G1} is the amount of gate charge per upper MOSFET at V_{GS1} gate-source voltage and N_{Q1} is the number of control (upper) MOSFETs. The ΔV_{BOOT_CAP} term is defined as the allowable droop in the rail of the upper gate drive. Select results are exemplified in Figure 4.

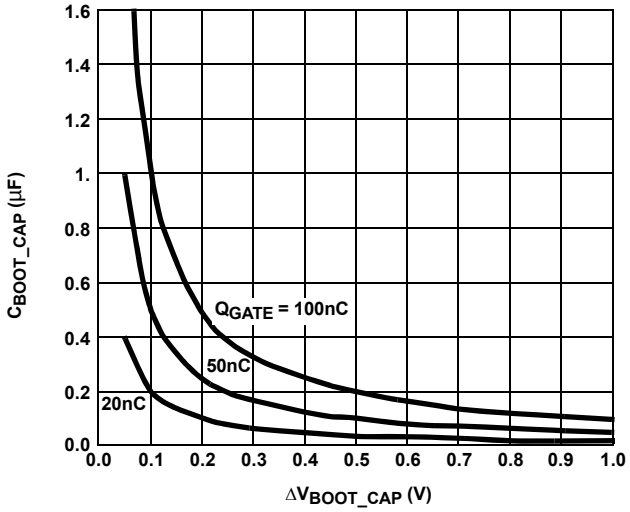


FIGURE 4. BOOTSTRAP CAPACITANCE vs BOOT RIPPLE VOLTAGE

Power Dissipation

Package power dissipation is mainly a function of the switching frequency (F_{SW}), the output drive impedance, the layout resistance, the selected MOSFET's internal gate resistance and its total gate charge (Q_G). Calculating the power dissipation in the driver for a desired application is critical to ensure safe operation. Exceeding the maximum allowable power dissipation level may push the IC beyond the maximum recommended operating junction temperature. The DFN package is more suitable for high frequency applications. See "Layout Considerations" on page 8 for thermal impedance improvement suggestions. The total driver power loss, essentially MOSFETs' gate charge and driver internal circuitry losses, can be estimated using Equations 2 and 3, respectively.

$$P_{Qg\_TOT} = P_{Qg\_Q1} + P_{Qg\_Q2} + I_Q \bullet VCC$$

$$P_{Qg\_Q1} = \frac{Q_{G1} \bullet UVCC^2}{V_{GS1}} \bullet F_{SW} \bullet N_{Q1} \qquad \text{(EQ. 2)}$$

$$P_{Qg\_Q2} = \frac{Q_{G2} \bullet LVCC^2}{V_{GS2}} \bullet F_{SW} \bullet N_{Q2}$$

$$I_{DR} = \left(\frac{Q_{G1} \bullet UVCC \bullet N_{Q1}}{V_{GS1}} + \frac{Q_{G2} \bullet LVCC \bullet N_{Q2}}{V_{GS2}}\right) \bullet F_{SW} + I_Q \qquad \text{(EQ. 3)}$$

where the gate charge (Q_{G1} and Q_{G2}) is defined at a particular gate to source voltage (V_{GS1} and V_{GS2}) in the corresponding MOSFET datasheet; I_Q is the driver's total quiescent current with no load at both drive outputs; N_{Q1} and N_{Q2} are number of upper and lower MOSFETs, respectively; UVCC and LVCC are the drive voltages for both upper and lower FETs, respectively. The I_Q*VCC product is the bias power of the driver without a load.

$$P_{DR} = P_{DR\_UP} + P_{DR\_LOW} + I_Q \bullet VCC$$

$$P_{DR\_UP} = \left(\frac{R_{HI1}}{R_{HI1} + R_{EXT1}} + \frac{R_{LO1}}{R_{LO1} + R_{EXT1}}\right) \bullet \frac{P_{Qg\_Q1}}{2}$$

$$P_{DR\_LOW} = \left(\frac{R_{HI2}}{R_{HI2} + R_{EXT2}} + \frac{R_{LO2}}{R_{LO2} + R_{EXT2}}\right) \bullet \frac{P_{Qg\_Q2}}{2} \quad \text{(EQ. 4)}$$

$$R_{EXT1} = R_{G1} + \frac{R_{GI1}}{N_{Q1}} \qquad R_{EXT2} = R_{G2} + \frac{R_{GI2}}{N_{Q2}}$$

The total gate drive power losses are dissipated among the resistive components along the transition path, as outlined in Equation 4. The drive resistance dissipates a portion of the total gate drive power losses, the rest will be dissipated by the external gate resistors (R_{G1} and R_{G2}) and the internal gate resistors (R_{GI1} and R_{GI2}) of MOSFETs. Figures 5 and 6 show the typical upper and lower gate drives turn-on current paths.

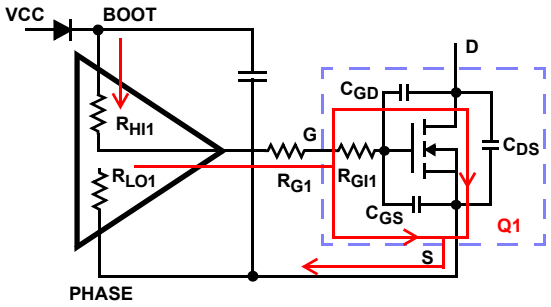


FIGURE 5. TYPICAL UPPER-GATE DRIVE TURN-ON PATH

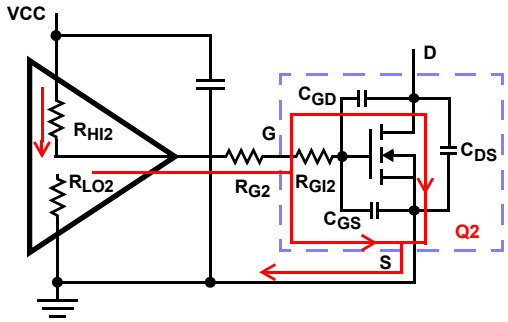


FIGURE 6. TYPICAL LOWER-GATE DRIVE TURN-ON PATH

Application Information

MOSFET and Driver Selection

The parasitic inductances of the PCB and of the power devices' packaging (both upper and lower MOSFETs) can cause serious ringing, exceeding absolute maximum rating of the devices. The negative ringing at the edges of the PHASE node could increase the bootstrap capacitor voltage through the internal bootstrap diode, and in some cases, it may overstress the upper MOSFET driver. Careful layout, proper selection of MOSFETs and packaging, as well as the driver can minimize such unwanted stress.

Layout Considerations

A good layout helps reduce the ringing on the switching (PHASE) node and significantly lower the stress applied to the MOSFETs as well as the driver. The following advice is meant to lead to an optimized layout:

- Keep decoupling circuit loops (VCC-GND and BOOT-PHASE) as short as possible.
- Minimize trace inductance, especially on low-impedance lines. All power traces (UGATE, PHASE, LGATE, GND, VCC) should be short and wide, as much as possible.
- Minimize the inductance of the PHASE node. Ideally, the source of the upper and the drain of the lower MOSFET should be as close as thermally allowable.
- Minimize the current loop of the output and input power trains. Short the source connection of the lower MOSFET to ground as close to the transistor pin as feasible. Input capacitors (especially ceramic decoupling) should be placed as close to the drain of upper and source of lower MOSFETs as possible.

In addition, connecting the thermal pad of the DFN package to the power ground through one or several vias is recommended for high switching frequency, high current applications. This is to improve heat dissipation and allow the part to achieve its full thermal potential.

Upper MOSFET Self Turn-On Effects at Startup

Should the driver have insufficient bias voltage applied, its outputs are floating. If the input bus is energized at a high dV/dt rate while the driver outputs are floating, due to self-coupling via the internal C_{GD} of the MOSFET, the gate of the upper MOSFET could momentarily rise up to a level greater than the threshold voltage of the device, potentially turning on the upper switch. Therefore, if such a situation could conceivably be encountered, it is a common practice to place a resistor (R_{UGPH}) across the gate and source of the upper MOSFET to suppress the Miller coupling effect. The value of the resistor depends mainly on the input voltage's rate of rise, the C_{GD}/C_{GS} ratio, as well as the gate-source threshold of the upper MOSFET. A higher dV/dt, a lower C_{GD}/C_{GS} ratio, and a lower gate-source threshold upper FET will require a smaller resistor to diminish the effect of the internal capacitive coupling. For most applications, the integrated 20kΩ resistor is sufficient, not measurably affecting normal performance and efficiency.

The coupling effect can be roughly estimated with Equation 5, which assumes a fixed linear input ramp and neglects the clamping effect of the body diode of the upper drive and the bootstrap capacitor. Other parasitic components, such as lead inductances and PCB capacitances are also not taken into account. Figure 7 provides a visual reference for this phenomenon and its potential solution.

$$V_{GS\_MILLER} = \frac{dV}{dt} \cdot R \cdot C_{rss}\left(1 - e^{\frac{-V_{DS}}{\frac{dV}{dt} \cdot R \cdot C_{iss}}}\right) \quad \text{(EQ. 5)}$$

$$R = R_{UGPH} + R_{GI} \qquad C_{rss} = C_{GD} \qquad C_{iss} = C_{GD} + C_{GS}$$

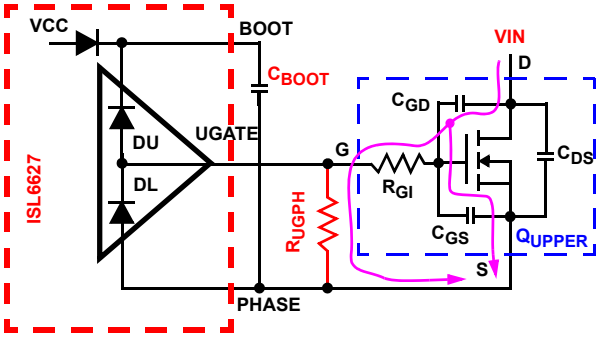


FIGURE 7. GATE TO SOURCE RESISTOR TO REDUCE UPPER MOSFET MILLER COUPLING

General PowerPAD Design Considerations

Figure 8 shows the recommended use of vias on the thermal pad to remove heat from the IC. This typical array populates the thermal pad footprint with vias spaced three times the radius distance from the center of each via. Small via size is advisable, but not to the extent that solder reflow becomes difficult.

All vias should be connected to the pad potential, with low thermal resistance for efficient heat transfer. Complete connection of the plated-through hole to each plane is important. It is not recommended to use “thermal relief” patterns to connect the vias.

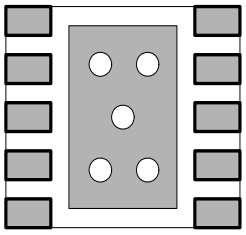


FIGURE 8. PCB VIA PATTERN

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest Rev.

DATE	REVISION	CHANGE
January 24, 2014	FN6992.1	On page 3 - added pin 10 to the description: PHASE - Connect this pin to the SOURCE of the upper MOSFET and the DRAIN of the lower MOSFET. This pin provides a return path for the upper gate drive. On page 10 - Updated "Products" verbiage to "About Intersil" verbiage On page 11 - Updated POD L10.3x3 from rev 6 to rev 9. Updates since rev 6: Removed package outline and included center to center distance between lands on recommended land pattern. Removed Note 4 "Dimension b applies to the metallized terminal and is measured between 0.18mm and 0.30mm from the terminal tip." since it is not applicable to this package. Renumbered notes accordingly. Corrected L-shaped leads in Bottom view and land pattern so that they align with the rest of the leads (L shaped leads were shorter). Added missing dimension 0.415 in Typical Recommended land pattern.
September 22, 2011	FN6992.0	Initial release.

About Intersil

Intersil Corporation is a leader in the design and manufacture of high-performance analog, mixed-signal and power management semiconductors. The company's products address some of the largest markets within the industrial and infrastructure, personal computing and high-end consumer markets. For more information about Intersil, visit our website at www.intersil.com.

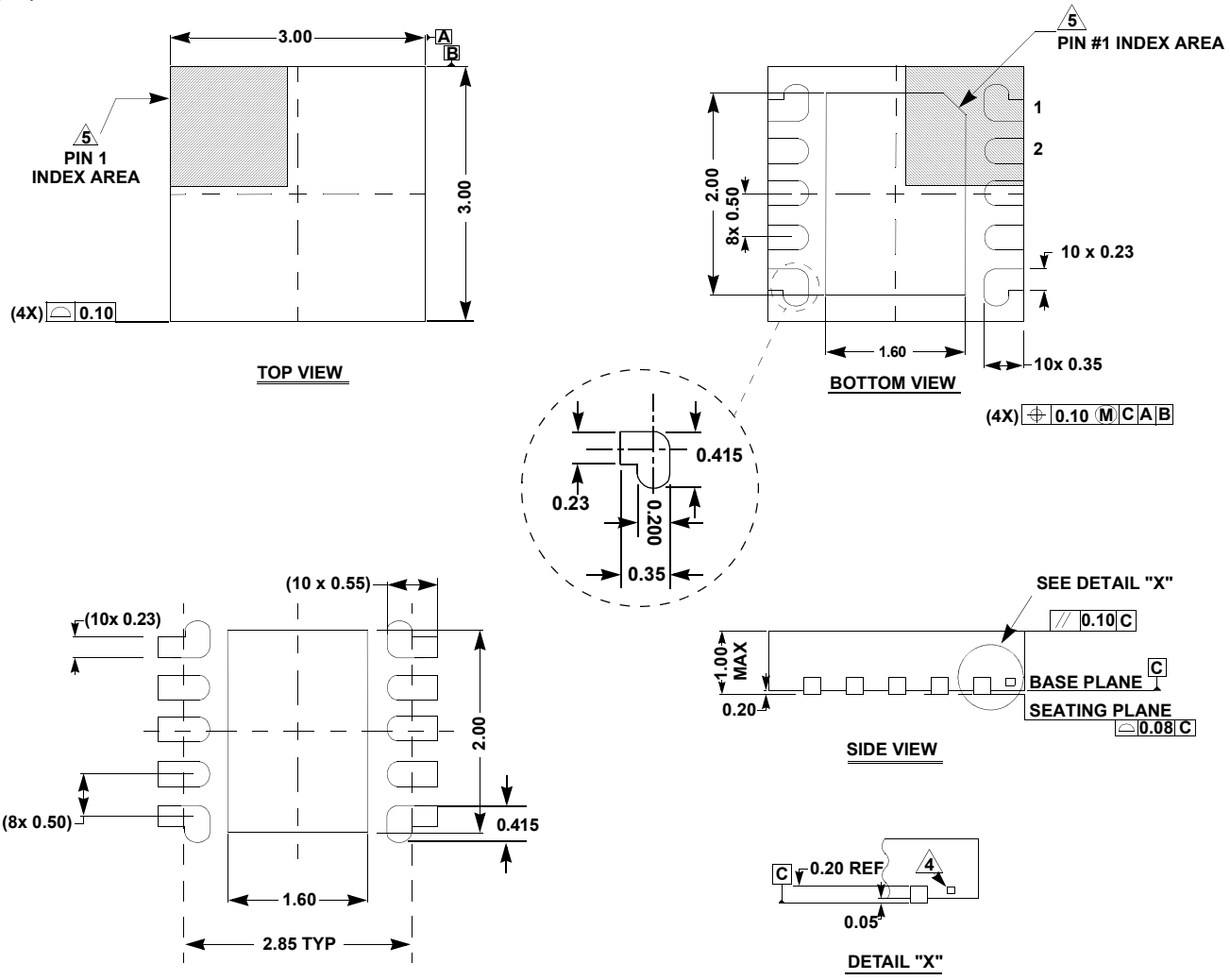
For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at www.intersil.com. You may report errors or suggestions for improving this datasheet by visiting www.intersil.com/en/support/ask-an-expert.html. Reliability reports are also available from our website at http://www.intersil.com/en/support/qualandreliability.html#reliability

Package Outline Drawing

L10.3x3

10 LEAD DUAL FLAT PACKAGE (DFN)

Rev 9, 10/13



NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Tiebar shown (if present) is a non-functional feature.
5. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.