Low Voltage Voice Coil Motor Driver

Features and Benefits

- WLCSP package for minimum footprint
- Ramp control circuit
- Fixed I²C logic thresholds
- 10-bit D-to-A converter
- 100 µA resolution
- Low voltage I²C serial interface
- Low current draw sleep mode-active low
- 2.3 to 5.5 V operation

Applications:

- Camera focus motor

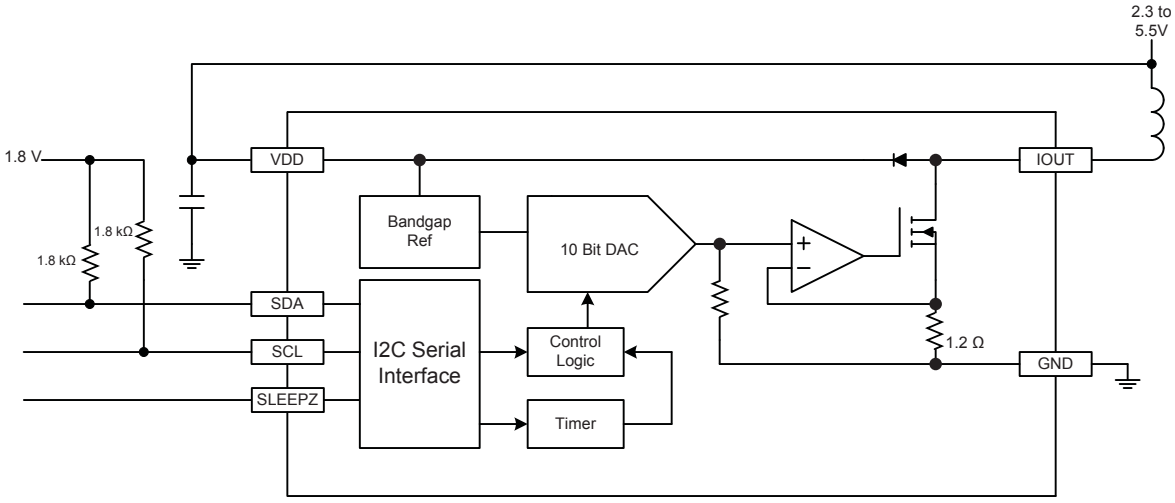
Package: 6-Bump Chip Scale Package (suffix CG)

Description

Designed for linear control of small form factor voice coil motors, the A3907 is capable of peak output currents to 102 mA and operating voltages to 5.5 V.

Internal circuit protection includes thermal shutdown with hysteresis, flyback clamp diode, and undervoltage monitoring of V_{DD}.

Functional Block Diagram



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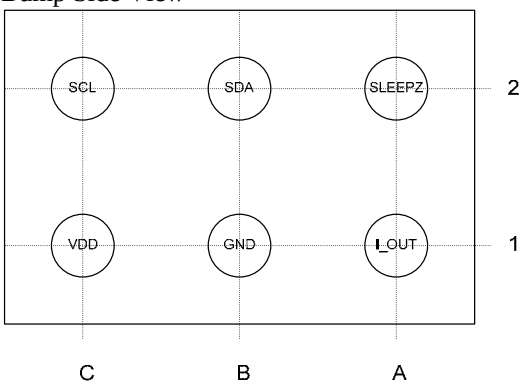
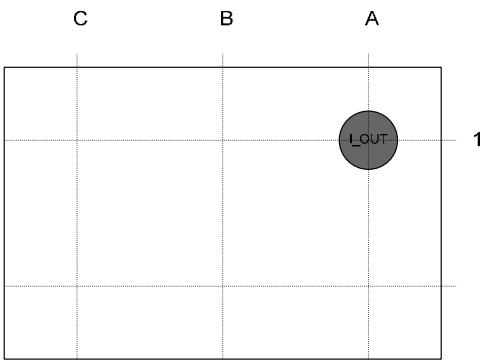
ABSOLUTE MAXIMUM RATINGS		Conditions	Min.	Typ	Max.	Units
Supply Voltage	V_{DD}				6	V
Logic Input Voltage Range	Vin		-.3		Vdd+.3	V
Junction Temperature	Tj				150	°C
Storage Temperature Range	Ts		-40		150	°C
Operating Temperature Range			-40		85	°C
Package Thermal Resistance						
A3907ECG	Rja	4 layer PCB		64		°C/W

Pin Name	Pin Description	
IOUT	Sink Drive Output	A1
SLEEPZ	Standby Mode Control	A2
GND	Ground	B1
SDA	I^2C data	B2
VDD	Power Supply In	C1
SCL	I^2C clock	C2

Bump Side View



Top Side View



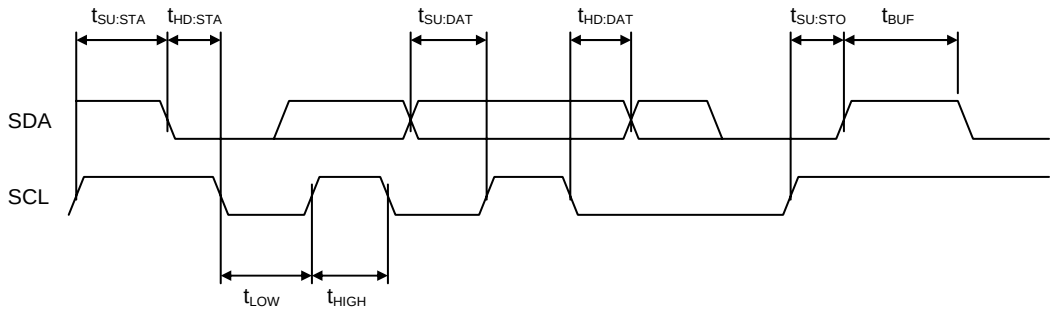
ELECTRICAL CHARACTERISTICS at T_A = 25°C, VDD = 2.3V to 5.5V (unless noted otherwise)

Characteristics	Sym	Test Conditions	Limits			
			Min.	Typ.	Max.	Units
Supply Current	I_{DD}		–	.5	2	mA
		Sleep Mode (SLEEPZ=Low) 2.3 to 3.5V	–	<100	500	nA
UVLO Enable Threshold	UVLOth	Vdd Rising		2	2.295	V
UVLO Hysteresis	UVLOhys		100			mV
Thermal Shutdown Temp.	T_{JTSD}	Temperature increasing.		165		°C
Thermal Shutdown Hysteresis	ΔT_J	Recovery = T_{JTSD} - ΔT_J		15		°C
Power Up Delay				10		uS
D/A						
Resolution		Target = 100uA/LSB		10		Bits
Relative Accuracy	INL	Code = 64 to 1023, Endpoint method		+/-4		LSB
Differential Nonlinearity	DNL	Guaranteed Monotonic.			+/-1	LSB
Max Output Current	Imax	Code=1023		102.3		mA
Gain Error		Tj = 25°C, Code 64 to 1023, VDD= 2.6V to 3.0V	-10	<3	10	%FS
Gain Error Drift (note 1)		Tj = -40°C to 125°C		.2		LSB/°C
Minimum Code Error	Ios1	Code = 1	0	1	5	mA
Offset Error	Ios	Code = 64		.5		mA
Output						
Slew Rate Timer	Ts	Relative to target value	-10		10	%
Output Voltage Range	Vout		.35		Vdd-.1	V
Output Rds(on)	Rds	Rsense + Rsink, Iout=102.3mA		1.45		ohm

1) Assured by design and characterization, not production tested.

ELECTRICAL CHARACTERISTICS at T_A = 25°C, VDD = 2.3V to 5.5 V (unless noted otherwise)

Characteristics	Symbol	Test Conditions	Limits			Units
			Min.	Typ.	Max.	
I^2C Interface						
Bus Free Time Between Stop/Start	t_{BUF}		1.3			µs
Hold Time Start Condition	$t_{HD:STA}$		.6			µs
Setup Time for Repeated Start Condition	$t_{SU:STA}$		.6			µs
SCL Low Time	t_{LOW}		1.3			µs
SCL high Time	t_{HIGH}		.6			µs
Data Setup Time	$t_{SU:DAT}$		100			ns
Data Hold Time	$t_{HD:DAT}$		0		900	ns
Setup Time for Stop Condition	$t_{SU:STO}$		.6			µs
Logic Input (SDA,SCL) Low Level	V_{IL}				0.84	V
Logic Input (SDA,SCL) High Level	V_{IH}		1.26			V
Sleep Input Low Level	Vinslp				.54	V
Sleep Input High Level	Vinslp		1.5			V
Input Hysteresis	V_{HYS}	SDA and SCL only		100		mV
Logic Input Current	I_{IN}	V_{IN} = 0V to Vdd	-1	0	1	µA
Output Voltage (SDA)	V_{OL}	I_{LOAD} = 1.5mA			0.36	V
SCL Clock Frequency	f_{CLK}		-		400	kHz
SDA Output Fall Time	t_{OF}	V_{IH} to V_{IL}	-		250	ns



Functional Description

The A3907 output current is controlled by programming the DAC value via the I^2C serial port. The target output current can be calculated by

I_out = DAC * 100uA …..where DAC = 1 to 1023

Code = 0 is a disable state for the output sink drive. The DAC will be set to code = 0 upon power up or fault condition on VDD.

SLEEPZ. A logic low input will disable all of the internal circuitry and prevent the IC from draining battery power.

Output Range. The voltage on the IOUT pin should be over TBDmV to guarantee the accuracy and linearity on the programmed current. The output voltage is a function of the battery voltage, motor resistance, and the programmed load current.

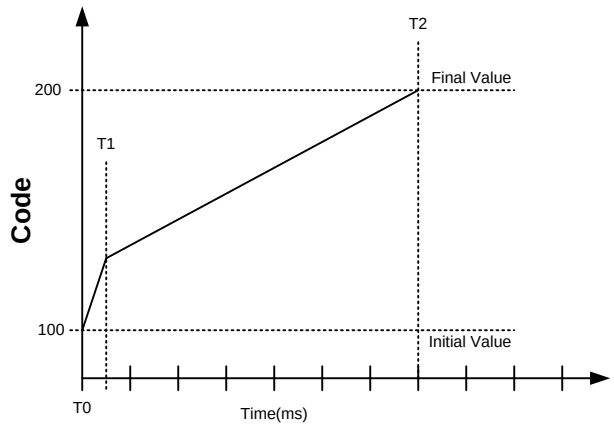
Clamp Diode. When the output is turned off the load inductance will cause the output voltage to rise. A clamp diode, from IOUT to VDD, is integrated in the IC to ensure the output voltage remains at a safe level.

Slew Rate Control. To allow flexibility on the change in current with respect to time 4 serial port bits are utilized to set the timing between the change between the present current level and the next current level programmed.

When a new current level is programmed, the 3907 will move to the new value by stepping through each of the intermediate current levels until it arrives at the final programmed value. The time between each step is adjustable according to the table below.

T3	T2	T1	T0	Step Method	Delay 1st Step	Delay 2nd Step
0	0	0	0	Single Step	0 (ramp feature disabled)	
0	0	0	1		6.25	
0	0	1	0		12.5	
0	0	1	1		25	
0	1	0	0		50	
0	1	0	1		100	
0	1	0	1		200	
0	1	1	0		0 (ramp feature disabled)	
0	1	1	1			
1	0	0	0	2 Step Method Switch over At Code = ABS(Programmed Code – Previous Code)/2	0 (ramp feature disabled)	
1	0	0	1		781ns	6.25us
1	0	1	0		781ns	12.5us
1	0	1	1		781ns	25us
1	1	0	0		781ns	50us
1	1	0	1		781ns	100us
1	1	1	0		781ns	200us
1	1	1	1		0 (ramp feature disabled)	

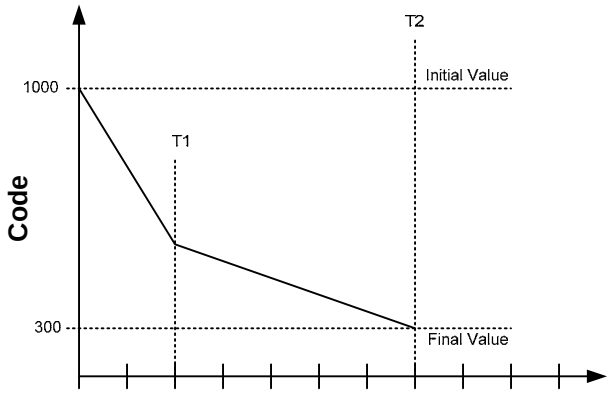
Example 1:



T3:T2:T1:T0 = 1100
Previous Code = 100
Programmed Code = 200

T1 = (200-100)/2)*781ns = 39uS
T2 –T1= 50*50uS = 2.5mS

Example 2:



T3:T2:T1:T0 = 1101
Previous Code = 1000
Programmed Code = 300

T1 = (1000-300)/2)*781ns = 273uS
T2 –T1= 350*100uS = 35mS

I²C Interface. This is a serial interface that uses two bus lines, SCL and SDA, to access the internal Control registers. Data is exchanged between a microcontroller (master) and the A3907 (slave). The clock input to SCL is generated by the master, while SDA functions as either an input or an open drain output, depending on the direction of the data. The I²C input thresolds do not depend on the VDD voltage of the A3907. The levels are fixed at approximately 1V. The fixed levels allow the SDA/SCL lines to be pulled up to a different logic level than the VDD supply of the 3907.

Timing Considerations

The control sequence of the communication through the I²C interface is composed of several steps in sequence:

1. **Start Condition**. Defined by a negative edge on the SDA line, while SCL is high.
2. **Address Cycle**. 7 bits of address, plus 1 bit to indicate write (0) or read(1), and an acknowledge bit. The address setting is 0x18, 0x1A, 0x1C or 0x1E.
3. **Data Cycles**.

Write - 8bits of data addressing internal control register, followed by an acknowledge bit.

4. **Stop Condition**. Defined by a positive edge on the SDA line, while SCL is high.

Except to indicate a Start or Stop condition, SDA must be stable while the clock is high. SDA can only be changed while SCL is low. It is possible for the Start or Stop condition to occur at any time during a data transfer. The A3907 always responds by resetting the data transfer sequence.

The Read/Write bit is set to low, to indicate a write cycle. Mulitple writes are allowed. If desired, the readback bit can be set to “1” to check what was last written.

The Acknowledge is used by the master to determine if the slave device is responding to its address and data. When the A3907 decodes the 7-bit address field as a valid address, it responds by pulling SDA low during the ninth clock cycle.

During a data write from the master, the A3907 pulls SDA low during the clock cycle that follows the data byte, in order to indicate that the data has been successfully received. In both cases, the master device must release the SDA line before the ninth clock cycle, in order to allow this handshaking to occur.

A3907 Slave Address

Device Identifier							R/W
0	0	0	1	1	X	X	0

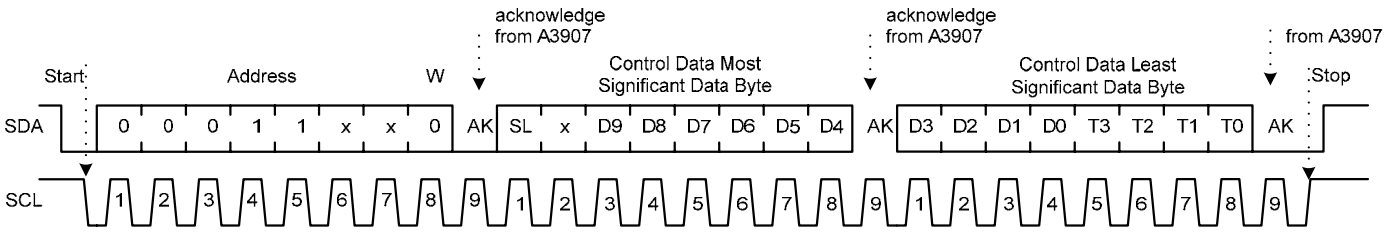
Control Register MSByte (I^2C Write register)

Bit	Name	Function
0	D4	DAC
1	D5	DAC
2	D6	DAC
3	D7	DAC
4	D8	DAC
5	D9	DAC MSB
6	T5	unused
7	SLEEP	1=Sleep 0=Normal Operation

Control Register LSByte (I^2C Write register)

Bit	Name	Function
0	T0	Time Setting LSB
1	T1	Time Setting Bit 1
2	T2	Time Setting Bit2
3	T3	Time Setting Bit 3
4	D0	DAC LSB
5	D1	DAC
6	D2	DAC
7	D3	DAC

Write Operation



Applications

Headroom. The current may not reach the programmed level if there is not adequate headroom in the output circuit. The IC output voltage must be over 350mV to guarantee normal linear operation. Vdd, Iload, Rload can be adjusted to ensure the device operates in the linear range. When the below equation is not satisfied the load current will be limited by the series impedance and may not reach the programmed level.

VDD(min) - Rload(max)*Iout(max) >= 350mV

Iout Errors Defined

Relative accuracy (INL):
This error is calculated by measuring the worse case deviation from a straight line defined from endpoints. The straight line endpoints are defined by the actual measured values at code=63 and code= 1023. See Figure A.

Differential nonlinearity (DNL) :
A measure of the monotonicity of the DAC. The slope of the line must always be positive for each incremental step.

DNL = [Iout(n+1) - Iout(n)]/LSB -1 LSB (n = 64 to 1023)

Offset error:
The measured output current at input code=64 compared to the ideal value according to the transfer function (6.4mA).

Gain Error:
The difference in the slopes of the ideal transfer function and the actual transfer function. The gain error is calculated by subtracting out the offset error at code 16 from the actual transfer function. This calculated value is compared to the ideal transfer function and reported as a percentage of the ideal full scale value (102.3mA). See Figure B.

Gain Error Drift:
Change in slope of the transfer function due to temperature, expressed as LSB/C.

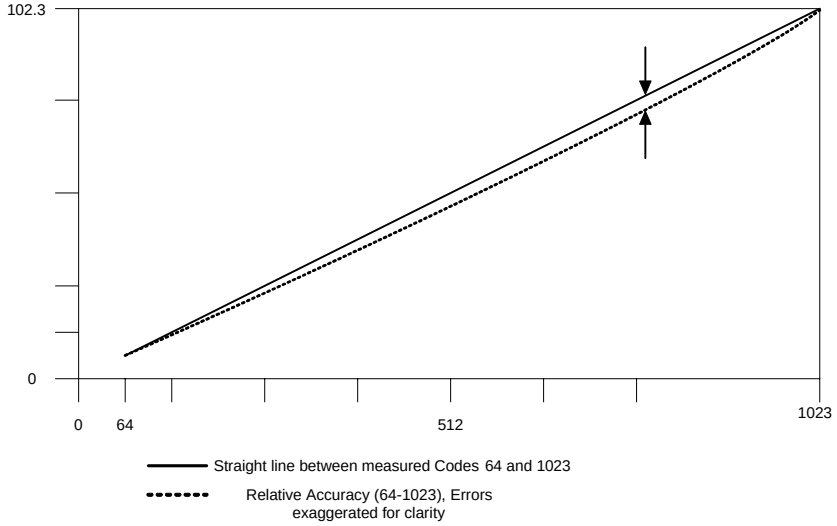


Figure A

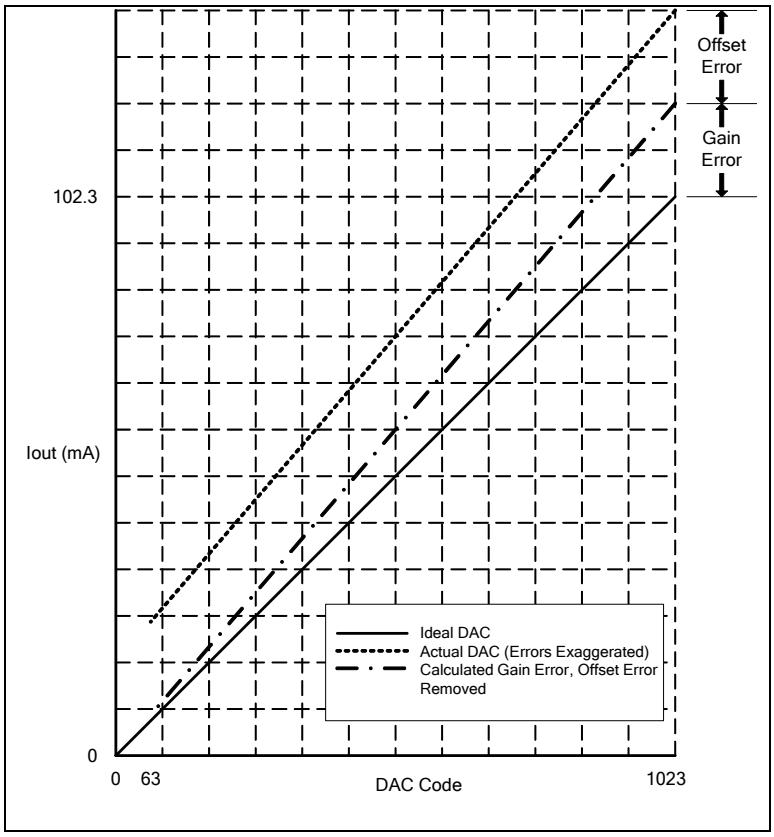
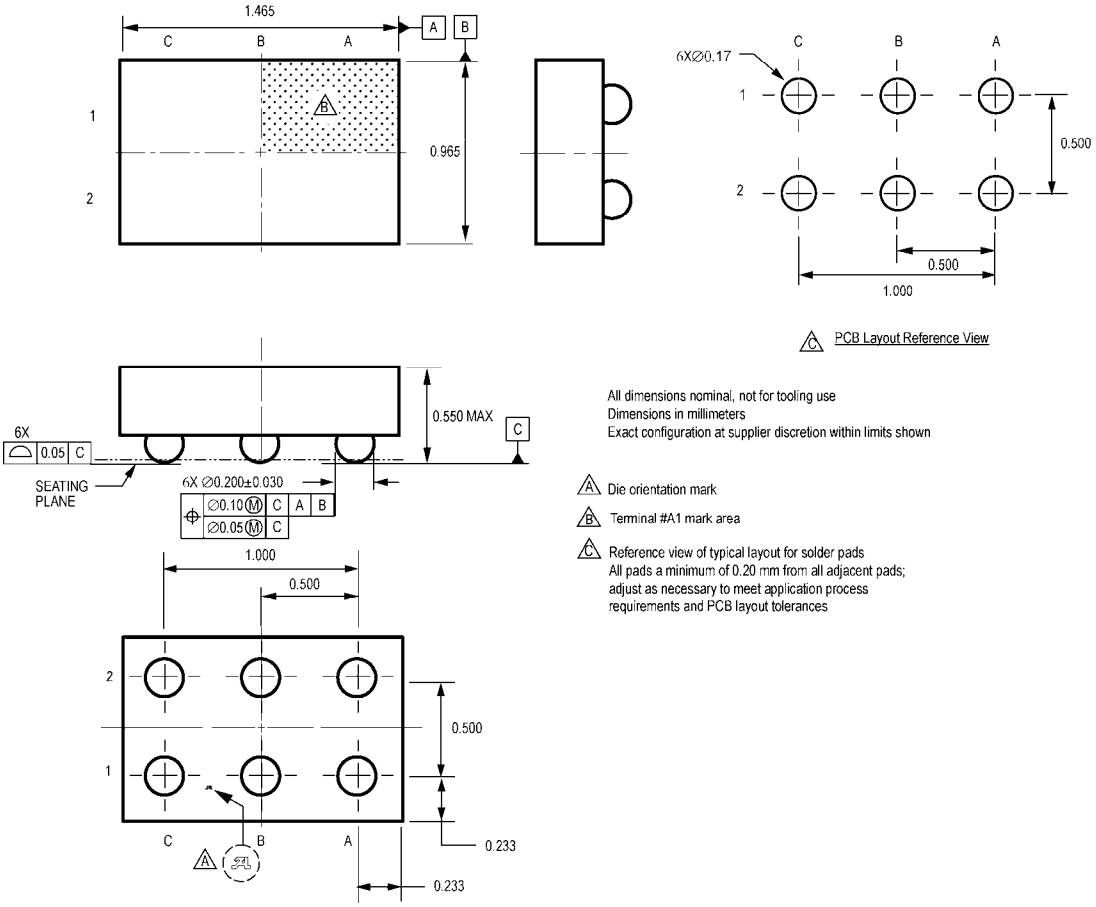


Figure B

WLCSP Package



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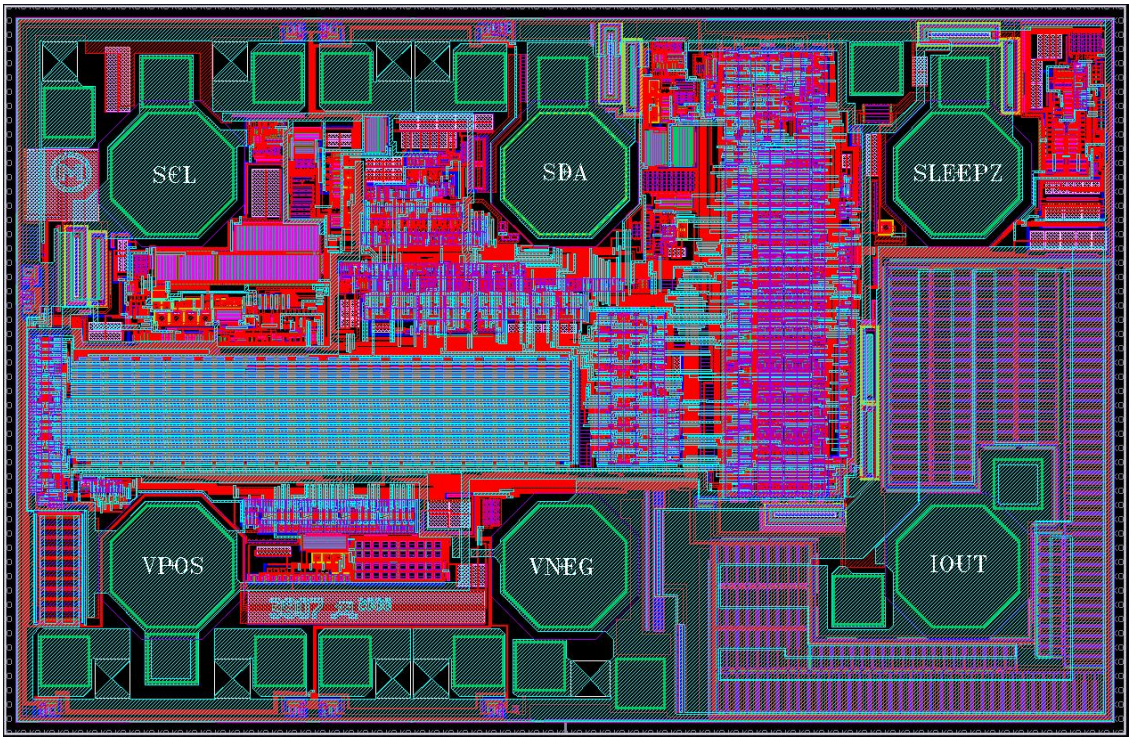
Pad Location:

Pin Name	Pin Description		Coordinates
VDD	Power Supply In	C1	X = -500 Y = -250
GND	Ground	B1	X = 0 Y = -250
IOUT	Sink Drive Output	A1	X = 500 Y = -250
SCL	I2C Clock	C2	X = -500 Y = 250
SDA	I2C Data	B2	X = 0 Y = 250
SLEEPZ	Standby Mode Control	A2	X = 500 Y = 250



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