30 W, Filterless, Class D, Output Sensing Audio Amplifier

Data Sheet

SSM3525

FEATURES

- Filterless digital input, mono Class D amplifier with Σ-Δ modulation
- Digitized output of output voltage, output current, and PV_{DD} supply voltage
- Operates from 4.5 V to 17 V supply, such as a 2-cell or 3-cell battery
- Input/output supply operation from 1.1 V to 1.98 V
- 30.2 W output power, 17 V supply and 4 Ω load at 1% THD + N
- 37.5 µV rms noise, 107 dB A weighted signal-to-noise ratio
- I^2C control with up to 4 pin-selectable addresses
- Multiple serial data formats
  - TDM, I^2S, or left justified slave
  - PDM input/output operating from 2.048 MHz to 6.144 MHz
- Support sample rates from 8 kHz to 192 kHz
- Flexible digital and analog gain adjustment
- AGC with battery voltage-based limiter
- 74 dB SNR on output current sensing and 85 dB SNR on voltage sensing
- 6.62 mA quiescent current at 12 V PV_{DD} supply
- Temperature sensor with 1°C readout
- Short-circuit, thermal protection, and thermal warning
- 23-ball, 2.26 mm × 2.38 mm, 0.4 mm pitch WLCSP
- Pop and click suppression
- User-selectable ultralow EMI emissions mode
- Power-on reset

APPLICATIONS

- Mobile computing
- Portable electronics

GENERAL DESCRIPTION

The SSM3525 is a fully integrated, high efficiency, mono Class D audio amplifier with digital input and digitized output of output voltage, output current, and PV_{DD} supply. The application circuit requires few external components and can operate from 4.5 V to 17 V (PV_{DD}) and 1.8 V (IOV_{DD}) supplies. It is capable of delivering 8.3 W of continuous output power into an 8 Ω load (or 15.3 W into 4 Ω) with <1% total harmonic distortion + noise (THD + N) from a 12 V supply, or 30.2 W into an 4 Ω load from a 17 V power supply, all with <1% THD + N.

The SSM3525 features a high efficiency, low noise modulation scheme that requires no external inductor/capacitor (LC) output filters. This scheme continues to provide high efficiency even at low output power. It operates with 92% efficiency at 9 W into an 8 Ω load, 12V or 89% efficiency at 20 W into 4 Ω from a 17 V supply, and it has an signal-to-noise ratio (SNR) of 107 dB, A weighted.

Spread spectrum pulse density modulation provides lower electromagnetic interference (EMI) radiated emissions compared with other Class D architectures, particularly above 100 MHz.

The digital input eliminates the need of an external digital-to-analog converter (DAC). The SSM3525 has a micropower shutdown mode with a typical shutdown current of 90 nA at 12 V PV_{DD} supply. Individual sense blocks can be powered down to save power when sense is not needed.

The device also includes pop and click suppression circuitry that minimizes voltage glitches at the output during turn on and turn off.

Current sensing is accomplished using an integrated analog-to-digital converter (ADC) and internal sense resistor. The digitized voltage and current information can be returned in various serial audio formats, including I^2S, time division multiplexing (TDM) and pulse density modulation (PDM).

The SSM3525 includes an integrated regulator to generate the required 5 V analog supply. Alternatively, if an external 5 V rail from a dc-to-dc converter is available, it can improve system efficiency.

The SSM3525 is designed to operate with an I^2C control interface and specified over the temperature range of −40°C to +85°C. It has built-in thermal shutdown and output short-circuit protection. It is available in a halide free, 23-ball, 2.26 mm × 2.38 mm wafer-level chip scale package (WLCSP).

Rev. A
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REVISION HISTORY

5/2018—Rev. 0 to Rev. A

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1/2018—Revision 0: Initial Version

FUNCTIONAL BLOCK DIAGRAM

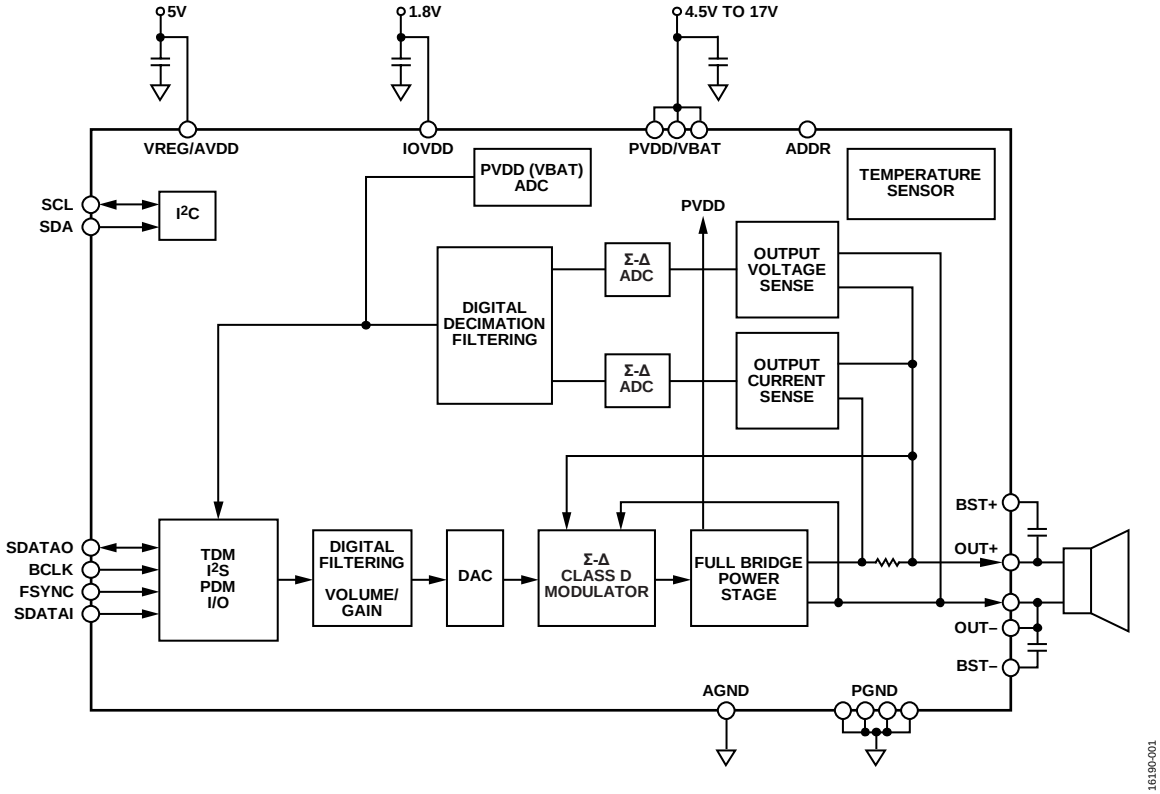

Figure 1. SSM3525 Block Diagram

SPECIFICATIONS

PV_{DD} = 12 V, AV_{DD} = 5 V (internal), IOV_{DD} = 1.8 V (external), R_L = 8 Ω + 33 µH, BCLK = 3.072 MHz, FSYNC = 48 kHz, −40°C to +85°C, unless otherwise noted. The measurements are taken with a 20 kHz AES17 low-pass filter. The other load impedances used are 4 Ω + 15 µH and 3 Ω +10 µH. The sine wave output powers above 20 W in 4 Ω cannot be continuous and might invoke the thermal limit indicator based on the power dissipation capability of the printed circuit board (PCB).

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
DEVICE CHARACTERISTICS						
Output Power/Channel	P_{OUT}	Frequency (f) = 1 kHz				
R_L = 8 Ω		THD + N = 1%, PV_{DD} = 17 V		15.2		W
		THD + N = 1%, PV_{DD} = 12 V		8.3		W
		THD + N = 1%, PV_{DD} = 7 V		2.8		W
		THD + N = 1%, PV_{DD} = 5 V		1.4		W
		THD + N = 10%, PV_{DD} = 17 V		18.7		W
		THD + N = 10%, PV_{DD} = 12 V		10.4		W
		THD + N = 10%, PV_{DD} = 7 V		3.5		W
		THD + N = 10%, PV_{DD} = 5 V		1.8		W
R_L = 4 Ω		THD + N = 1%, PV_{DD} = 17 V		30.2		W
		THD + N = 1%, PV_{DD} = 12 V		15.3		W
		THD + N = 1%, PV_{DD} = 7 V		5.2		W
		THD + N = 1%, PV_{DD} = 5 V		2.7		W
		THD + N = 10%, PV_{DD} = 17 V		37.2		W
		THD + N = 10%, PV_{DD} = 12 V		19.1		W
		THD + N = 10%, PV_{DD} = 7 V		6.6		W
		THD + N = 10%, PV_{DD} = 5 V		3.3		W
Efficiency	η	P_{OUT} = 9 W, R_L = 8 Ω, PV_{DD} = 12 V		92.1		%
		P_{OUT} = 9 W, R_L = 8 Ω, PV_{DD} = 12 V (low EMI mode)		92		%
		P_{OUT} = 20 W, R_L = 4 Ω, PV_{DD} = 17 V		89		%
		P_{OUT} = 20 W, R_L = 4 Ω, PV_{DD} = 17 V (low EMI mode)		88.8		%
Total Harmonic Distortion + Noise	THD + N	P_{OUT} = 5 W, R_L = 8 Ω, f = 1 kHz, PV_{DD} = 16 V		0.004	0.01	%
Load Inductance			5			µH
Output FET On Resistance	R_{ON}			110		mΩ
OverCurrent Protection Trip Point	I_{OC}		6			A_{PEAK}
Average Switching Frequency	f_{SW}			300		kHz
Differential Output Offset Voltage	V_{OOS}	Gain = 8.9V/V			±5.0	mV
POWER SUPPLIES						
Supply Voltage Range	PV_{DD}	Guaranteed from PSRR test	4.5		17	V
	AV_{DD}		4.5	5.0	5.5	V
	IOV_{DD}	I^2S/TDM operation	1.1	1.80	1.98	V
Power Supply Rejection Ratio (AC)	$PSRR_{AC}$	V_{RIPPLE} = 1 V rms at 1 kHz		87	73	dB
GAIN CONTROL		Measured with 0 dBFS input at 1 kHz, no load				
Output Voltage Peak		Analog gain setting = 6.3 V/V with PV_{DD} = 6.3 V		6.3		V_{PEAK}
		Analog gain setting = 8.9 V/V with PV_{DD} = 8.9 V		8.9		V_{PEAK}
		Analog gain setting = 12.6 V/V with PV_{DD} = 12.6 V		12.6		V_{PEAK}
		Analog gain setting = 16.0 V/V with PV_{DD} = 16 V		16		V_{PEAK}
PDM Input Gain		PDM input density for full-scale output		0.5		FS

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
SHUTDOWN CONTROL						
Turn-On Time	t_{WU}	I^2S mode		10		ms
Turn-Off Time	t_{SD}			500		µs
Output Impedance	Z_{OUT}		100			kΩ
NOISE PERFORMANCE[1]						
Output Voltage Noise	e_n	f = 20 Hz to 20 kHz, A weighted, PV_{DD} = 12 V		37.5		µV rms
		f = 20 Hz to 20 kHz, A weighted, PV_{DD} = 17 V		48		µV rms
Signal-to-Noise Ratio	SNR	P_{OUT} = 8.2 W, R_L = 8 Ω, A weighted, PV_{DD} = 12 V		107		dB
		P_{OUT} = 31 W, R_L = 4 Ω, A weighted, PV_{DD} = 17 V		107		dB
OUTPUT SENSING						
Output Sampling Rate (TDM)	fs	FSYNC pulse rate	8		192	KHz
PDM Gain Mapping		Voltage to current (V/I) sense PDM output with full-scale input		0.71		FS
Voltage Sense Signal-to-Noise Ratio	SNR_V			85		dB
Voltage Sense Full-Scale	V_{FS}	Output voltage at 0 dBFS output from ADC		±18		V_{PEAK}
Voltage Sense Absolute Accuracy		Temperature = 0°C to 70° C, output >−40 dBFS		±1.5		%
Voltage Sense Gain Drift		Temperature = 0°C to 70° C, output >−40 dBFS		0.5		%
Current Sense SNR	SNR_I			74		dB
Current Sense Full-Scale	$I_{SENSE,FS}$	Peak current with 0 dBFS output from ADC		6.96		A_{PEAK}
Current Sense Absolute Accuracy		Temperature = 0°C to 70° C, output >−40 dBFS		±2		%
Current Sense Gain Drift		Temperature = 0°C to 70° C, output >−40 dBFS		±0.5		%
Voltage Sense over Current Sense Ratio Drift		Temperature = 0°C to 70° C, output >−40 dBFS		±0.5		%
PV_{DD} Sense Full-Scale Range	PV_{FS}	PV_{DD} with full-scale ADC output	4		18	V
PV_{DD} Sense Absolute Accuracy		Temperature = 0°C to 70°C		3		LSBs
Current and Voltage Sense Linearity		From −40 dBr to 0 dBr		±0.5		dB

[1] The noise performance minimum and maximum limits are based on the bench data for −40°C to +85°C.

Software master power-down indicates the clocks are turned off. Auto power-down indicates there is no dither or zero input signal with clocks on; the device enters soft power-down after 2048 cycles of zero input values. Quiescent indicates triangular dither with zero input signal. All specifications are typical, with a 48 kHz sample rate, unless otherwise noted.

Table 2. Power Supply Current Consumption[1]

Edge Rate Control Mode	Register REG_EN Bit	Test Conditions	No Load					4 Ω + 15 µH					8 Ω +33 µH					Unit
			I_{PVDD}			I_{IOVDD}	I_{AVDD}	I_{PVDD}			I_{IOVDD}	I_{AVDD}	I_{PVDD}			I_{IOVDD}	AVDD	
			5 V	12 V	17 V	1.8 V	5 V	5 V	12 V	17 V	1.8 V	5 V	5 V	12 V	17 V	1.8 V	5 V	
Normal	0	Software master power-down	0.09	0.09	0.09	8.01	3.24	0.09	0.09	0.09	8.01	3.24	0.09	0.09	0.09	8.01	3.24	µA
		Quiescent (all ADCs on)	1.73	3.43	4.49	0.992	5.14	1.96	3.55	4.61	0.994	5.26	1.67	3.29	4.49	0.995	5.14	mA
		Quiescent (all ADCs off)	1.74	3.44	4.51	0.817	3.28	1.96	3.54	4.61	0.816	3.44	1.67	3.29	4.49	0.82	3.34	mA
	1	Software master power-down	0.09	0.09	0.09	8.01	N/A	0.09	0.09	0.09	8.01	N/A	0.09	0.09	0.09	8.01	N/A	µA
		Quiescent (all ADCs on)	6.86	8.56	9.65	0.995	N/A	6.81	8.61	10.21	0.998	N/A	6.83	8.51	9.79	0.996	N/A	mA
		Quiescent (all ADCs off)	5.04	6.73	7.86	0.821	N/A	4.98	6.75	8.44	0.766	N/A	5.01	6.69	7.96	0.817	N/A	mA
Low EMI	0	Software master power-down	0.09	0.09	0.09	8.01	3.24	0.09	0.09	0.09	8.01	3.24	0.09	0.09	0.09	8.01	3.24	µA
		Quiescent (all ADCs on)	1.663	3.35	4.48	0.991	5.08	1.6	3.35	4.68	0.994	5.21	1.59	3.28	4.48	0.996	5.09	mA
		Quiescent (all ADCs off)	1.663	3.35	4.58	0.823	3.28	1.6	3.37	4.71	0.819	3.41	1.59	3.25	4.48	0.819	3.27	mA
	1	Software master power-down	0.09	0.09	0.09	8.01	N/A	0.09	0.09	0.09	8.01	N/A	0.09	0.09	0.09	8.01	N/A	µA
		Quiescent (all ADCs on)	6.73	8.46	9.8	0.998	N/A	6.71	8.56	10.02	0.995	N/A	6.72	8.45	9.61	0.992	N/A	mA
		Quiescent (all ADCs off)	4.91	6.62	7.97	0.823	N/A	4.89	6.74	8.19	0.816	N/A	4.89	6.58	7.81	0.821	N/A	mA

[1] N/A means not applicable.

Table 3. Digital Input/Output

Parameter	Min	Typ	Max	Unit
HIGH INPUT VOLTAGE (V_{IH})				
BCLK, FSYNC, SDATAI, and SDATAO	0.7 × IOV_{DD}		1.98	V
SCL and SDA	0.7 × IOV_{DD}		5.5	V
LOW INPUT VOLTAGE (V_{IL})				
BCLK, FSYNC, SDATAI, SDATAO, SDA, SCL	−0.3		0.3 × IOV_{DD}	V
ADDR	−0.3		IOV_{DD} + 0.3	V
INPUT LEAKAGE				
HIGH (I_{IH})			1	µA
LOW (I_{IL})			1	µA
INPUT CAPACITANCE			5	pF
OUTPUT DRIVE STRENGTH (SDATAO)		3		mA

TIMING SPECIFICATIONS

Table 4. I²C Port Timing

Parameter	Min	Max	Unit	Description
I²C PORT				
f_{SCL}		1	MHz	SCL frequency
t_{SCLH}	0.26		µs	SCL high
t_{SCLL}	0.5		µs	SCL low
t_{SCS}	0.26		µs	Setup time; relevant for repeated start condition
t_{SCH}	0.26		µs	Hold time; after this period, the first clock is generated
t_{DS}	50		ns	Data setup time
t_{SCR}		120	ns	SCL rise time
t_{SCF}		120	ns	SCL fall time
t_{SDR}		120	ns	SDA rise time
t_{SDF}		120	ns	SDA fall time
t_{BFT}	0.5		µs	Bus-free time (time between stop and start)

Table 5. Serial Port Digital Input Timing (I^2S/TDM Operation Modes Only)

Parameter	Min	Max	Unit	Description
SERIAL PORT				
t_{BIL}	8		ns	BCLK low pulse width
t_{BIH}	8		ns	BCLK high pulse width
t_{SIS}	4		ns	SDATAI setup time to BCLK rising edge
t_{SIH}	4		ns	SDATA hold time from BCLK rising edge
t_{LIS}	5		ns	FSYNC setup time to BCLK rising edge
t_{LIH}	5		ns	FSYNC hold time to BCLK rising edge
t_{BP}	20		ns	Minimum BCLK period

Table 6. Serial Port Digital Output Timing (I^2S/TDM Operation Modes Only)

Parameter	Min	Max	Unit	Description
SERIAL PORT				
t_{BIL}	8		ns	BCLK low pulse width.
t_{BIH}	8		ns	BCLK high pulse width.
t_{SIS}	4		ns	SDATAO setup time to BCLK rising edge
t_{SIH}	4		ns	SDATA hold time from BCLK rising edge
t_{LIS}	5		ns	FSYNC setup time to BCLK rising edge
t_{LIH}	5		ns	FSYNC hold time to BCLK rising edge
t_{BP}	20		ns	Minimum BCLK period

Table 7. PDM Timing Parameters

	Limit			
Parameter	Min	Max	Unit	Description
PDM Clock Frequency	2.048	6.144	MHz	
t_{FALL}		10	ns	Clock fall time
t_{RISE}		10	ns	Clock rise time
t_{SETUP}	10		ns	Data setup time
t_{HOLD}	7		ns	Data hold time

Digital Timing Diagrams

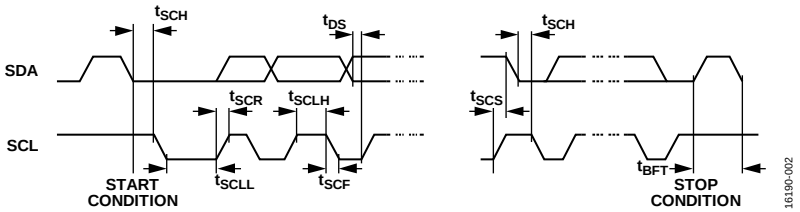

Figure 2. I^2C Port Timing

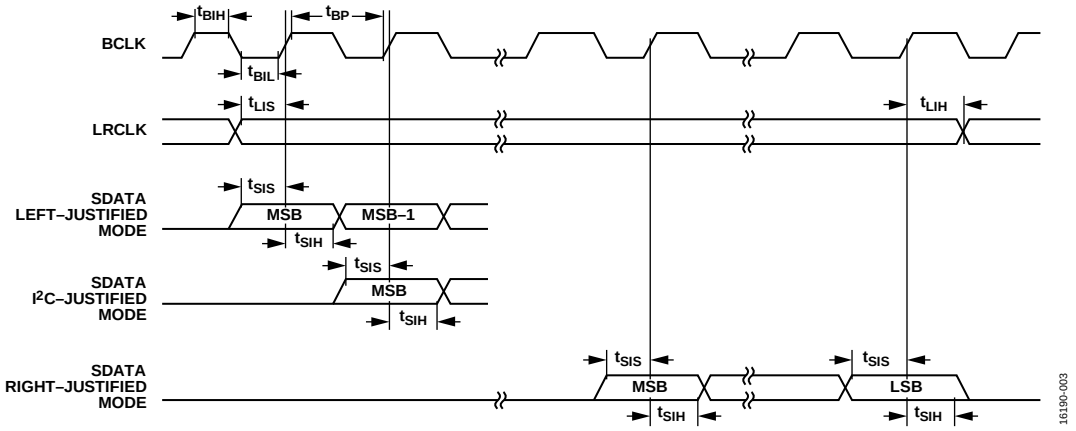

Figure 3. Serial Port SDATAI and SDATAO Timing

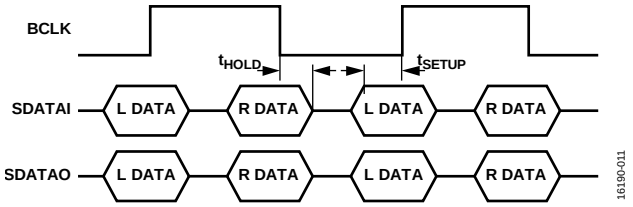

Figure 4. PDM Input/Output Format

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings apply at 25°C, unless otherwise noted.

Table 8.

Parameter	Rating
PV_{DD} Supply Voltage	−0.3 V to +18 V
IOV_{DD} Supply Voltage	−0.3 V to +1.98 V
AV_{DD} Supply Voltage	−0.3 V to +5.5 V
PGND and AGND Differential	±0.3 V
BCLK, FSYNC, ADDR, SDATAI Input Voltage	−0.3 V to +1.98 V
SCL and SDA Input Voltage	−0.3 V to +5.5 V
Electrostatic Discharge (ESD) Susceptibility, HBM 1.5 kΩ, 100 pF, JEDEC JS-001-2014	±1.5 kV
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +85°C
Junction Temperature Range	−65°C to +165°C
Lead Temperature Range (Soldering, 60 sec)	300°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to PCB design and operating environment. Careful attention to PCB thermal design is required. θ_{JA} and θ_{JB} are determined according to JESD51-9 on a 4-layer PCB with natural convection cooling.

Table 9. Thermal Resistance

Package Type	θ_{JA}[1]	θ_{JB}[1]	Unit
23-ball, 2.22 mm × 2.34 mm WLCSP	64.6	21.9	°C/W

[1] Thermal impedance simulated values are based on JEDEC2S2P thermal test board with two thermal vias. See JEDEC JESD51.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

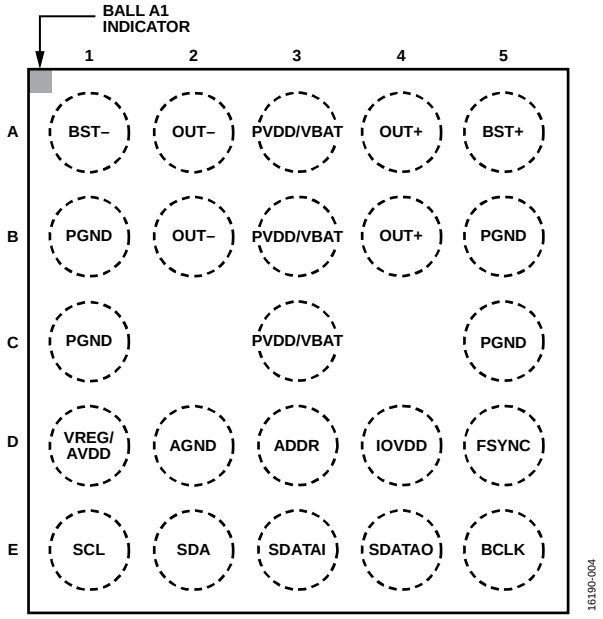

Figure 5. Ball Configuration (Top Side View)

Table 10. Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Description
A1	BST–	AIN	Bootstrap Capacitor, Inverting Output.
A2	OUT–	AOUT	Inverting Output.
A3, B3, C3	PVDD/VBAT	PWR	Power Stage Supply/Battery Supply.
A4	OUT+	AOUT	Noninverting Output.
A5	BST+	AIN	Bootstrap Capacitor, Noninverting Output.
B1, B5, C1, C5	PGND	PWR	Power Stage Ground.
B2	OUT–	AOUT	Inverting Output.
B4	OUT+	AOUT	Noninverting Output.
D1	VREG/AVDD	AIO	Analog Input/Output. 5 V regulator output/AVDD input.
D2	AGND	PWR	Analog Ground.
D3	ADDR	DIN	Address Selection.
D4	IOVDD	PWR	Input/Output and Digital Supply.
D5	FSYNC	DIN	Frame Sync Input.
E1	SCL	DIN	I^2C Clock.
E2	SDA	DIO	I^2C Data.
E3	SDATAI	DIN	I^2S/TDM Serial Data Input or PDM Data Input.
E4	SDATAO	DOUT	I^2S/TDM Serial Data Output or PDM Data Output.
E5	BCLK	DIN	TDM/I^2S Bit Clock Input, PDM Clock Input

[1] AOUT is analog output, PWR is power supply or ground pin, AIN is analog input, DIN is digital input, DOUT is digital output, and DIO is digital input/output.

TYPICAL PERFORMANCE CHARACTERISTICS

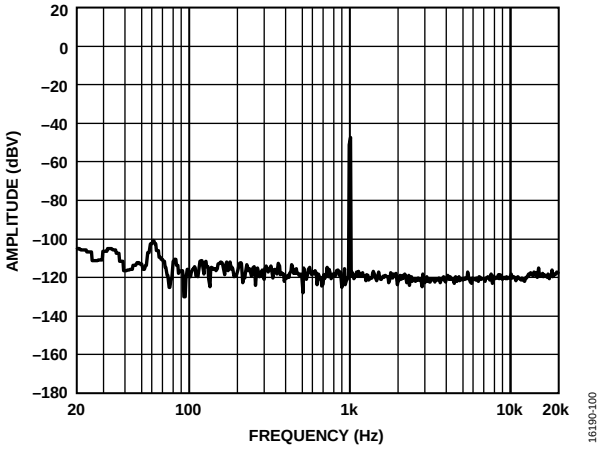

Figure 6. Fast Fourier Transform (FFT), –60 dBFS Input, Analog Gain = 6.3, R_L = 4 Ω

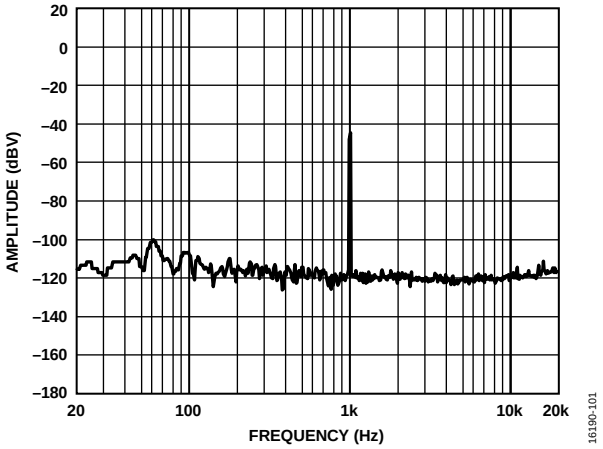

Figure 7. FFT, –60 dBFS Input, Analog Gain = 8.9, R_L = 4 Ω

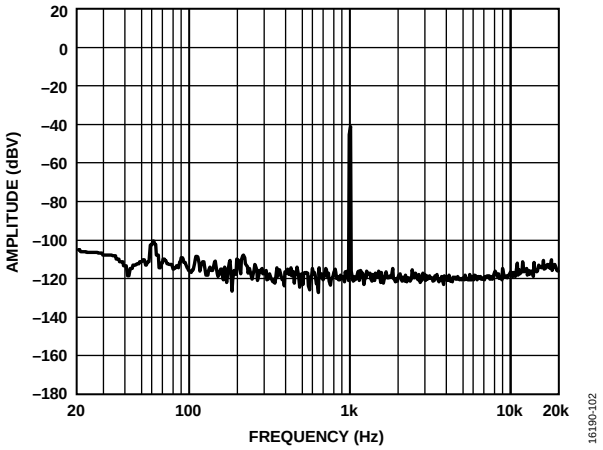

Figure 8. FFT, –60 dBFS Input, Analog Gain = 12.6, R_L = 4 Ω

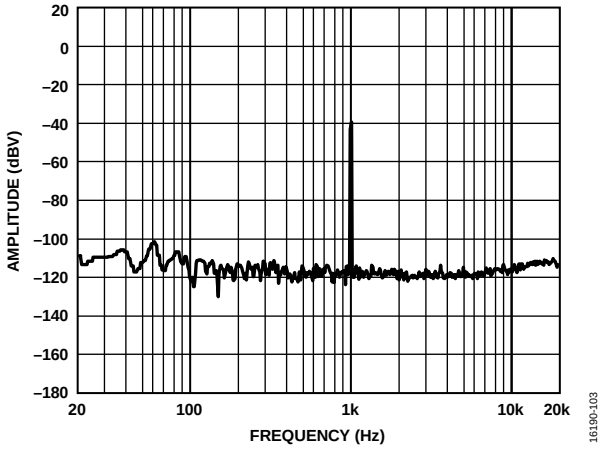

Figure 9. FFT, –60 dBFS Input, Analog Gain = 16, R_L = 4 Ω

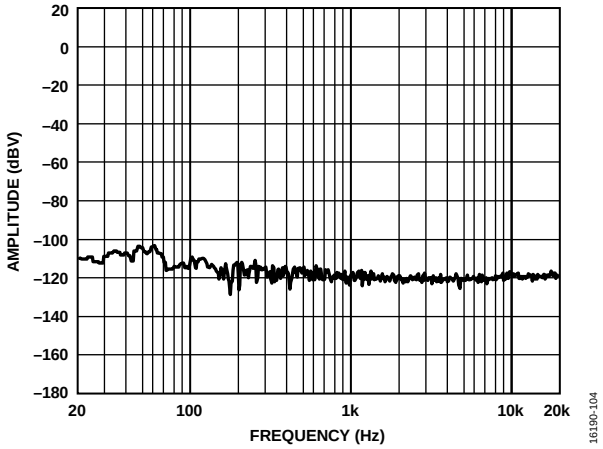

Figure 10. FFT, No Signal, Analog Gain = 6.3, R_L = 4 Ω

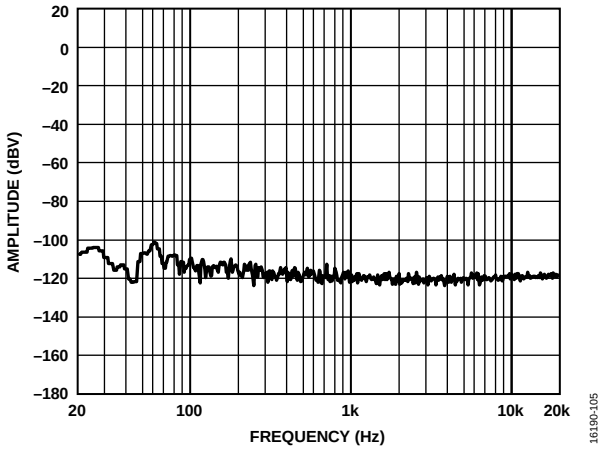

Figure 11. FFT, No Signal, Analog Gain = 8.9, R_L = 4 Ω

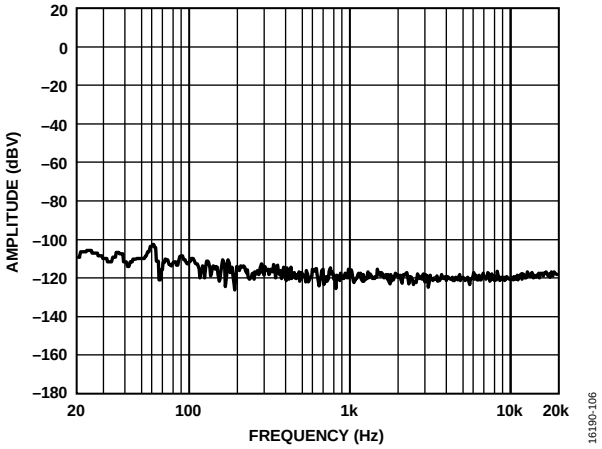

Figure 12. FFT, No Signal, Analog Gain = 12.6, R_L = 4 Ω

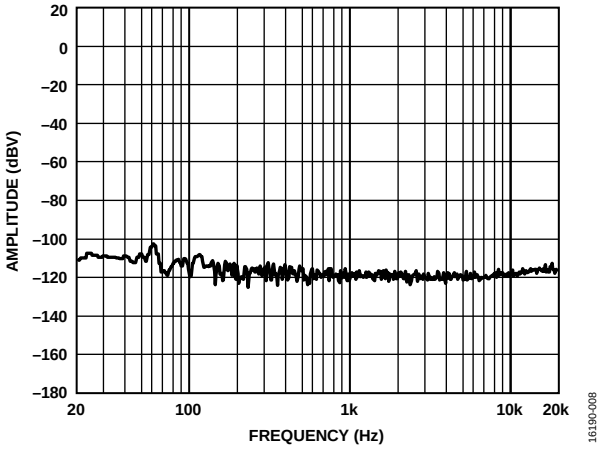

Figure 13. FFT, No Signal, Analog Gain = 16, R_L = 4 Ω

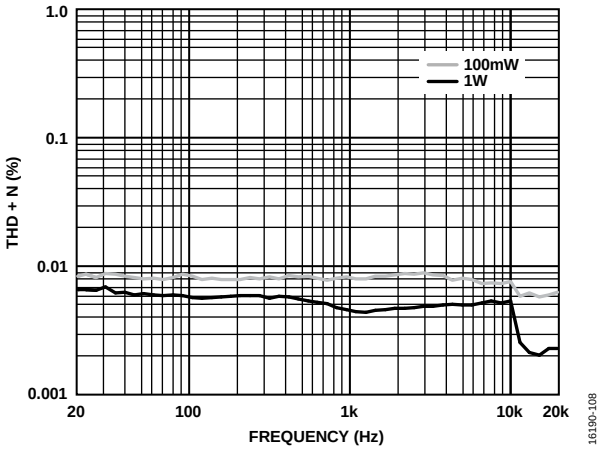

Figure 14. THD + N vs. Frequency into R_L = 4 Ω, PV_{DD} = 4.5 V

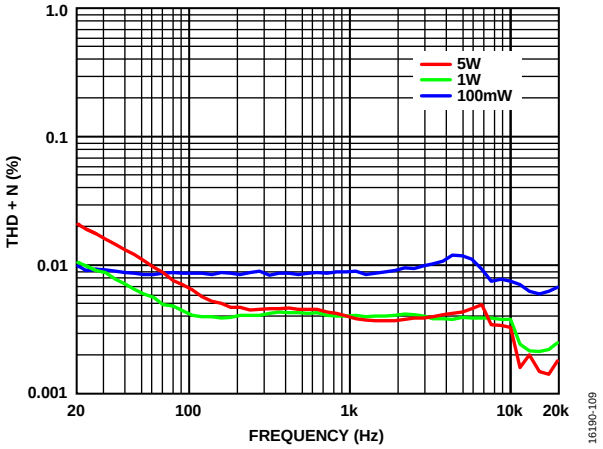

Figure 15. THD + N vs. Frequency into R_L = 4 Ω, PV_{DD} = 12 V

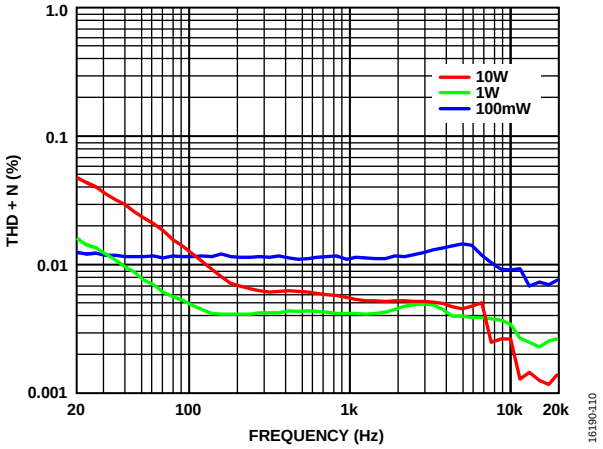

Figure 16. THD + N vs. Frequency into R_L = 4 Ω, PV_{DD} = 17 V

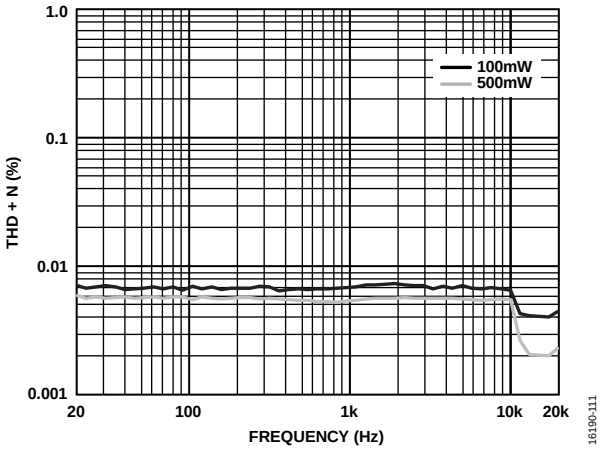

Figure 17. THD + N vs. Frequency into R_L = 8 Ω, PV_{DD} = 4.5 V

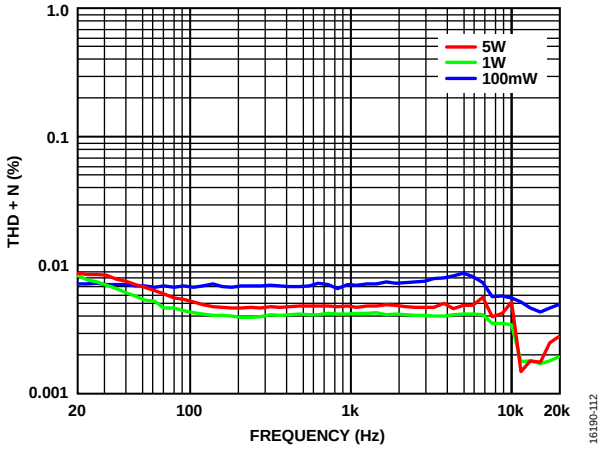

Figure 18. THD + N vs. Frequency into R_L = 8 Ω, PV_{DD} = 12 V

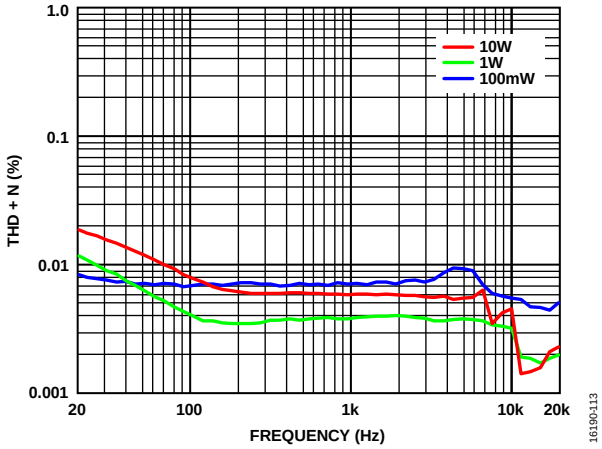

Figure 19. THD + N vs. Frequency into R_L = 8 Ω, PV_{DD} = 17 V

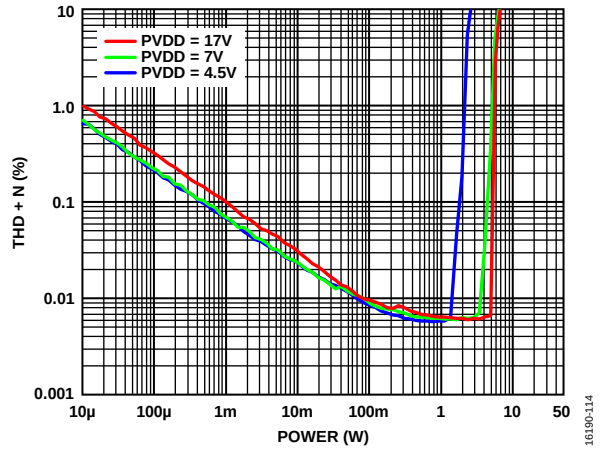

Figure 20. THD + N vs. Output Power, R_L = 4 Ω, Analog Gain = 6.3

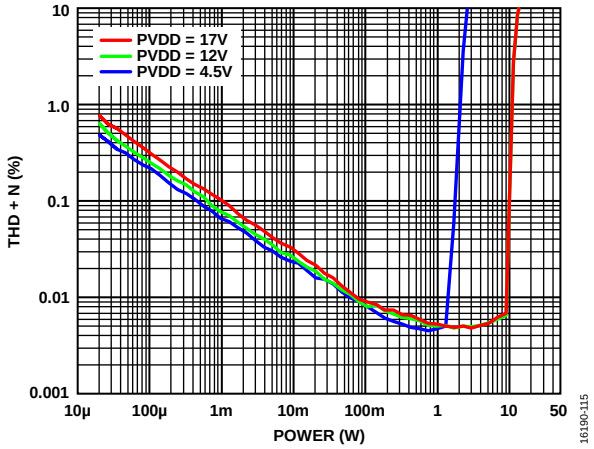

Figure 21. THD + N vs. Output Power, R_L = 4 Ω, Analog Gain = 8.9

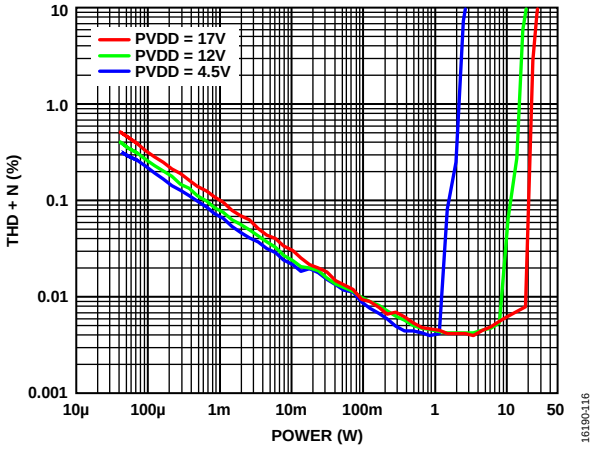

Figure 22. THD + N vs. Output Power, R_L = 4 Ω, Analog Gain = 12.6

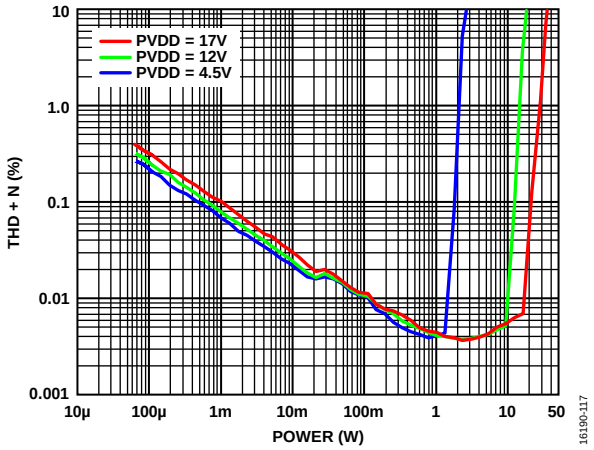

Figure 23. THD + N vs. Output Power, R_L = 4 Ω, Analog Gain = 16

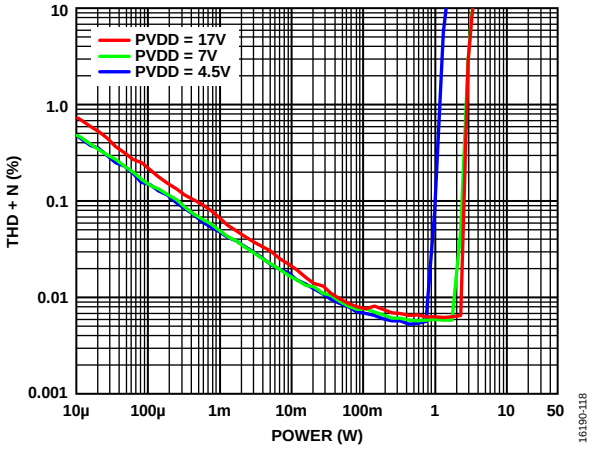

Figure 24. THD + N vs. Output Power, R_L = 8 Ω, Analog Gain = 6.3

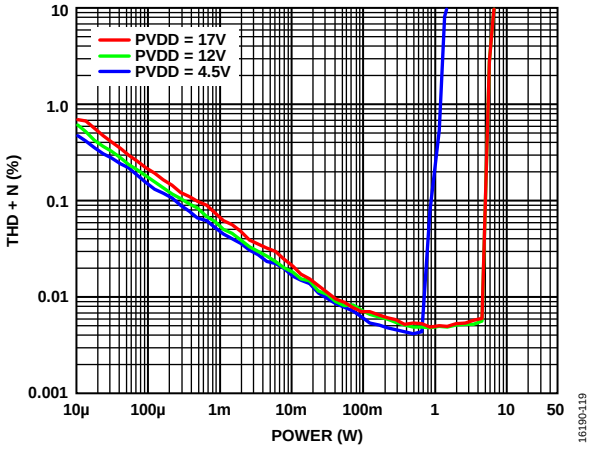

Figure 25. THD + N vs. Output Power, R_L = 8 Ω, Analog Gain = 8.9

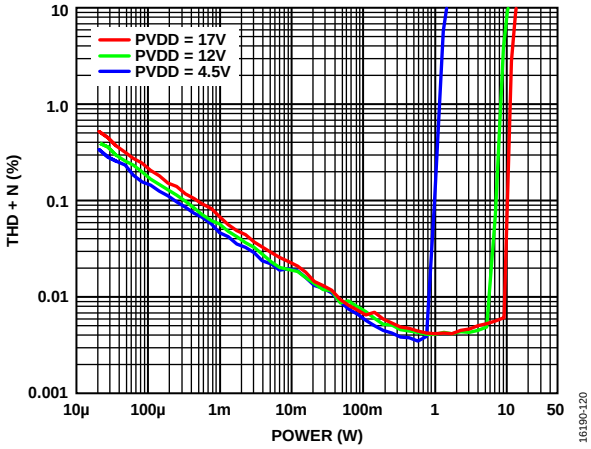

Figure 26. THD + N vs. Output Power, R_L = 8 Ω, Analog Gain = 12.6

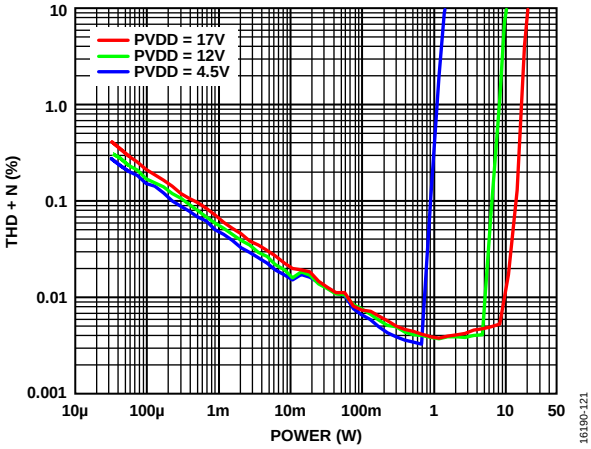

Figure 27. THD + N vs. Output Power, R_L = 8 Ω, Analog Gain = 16

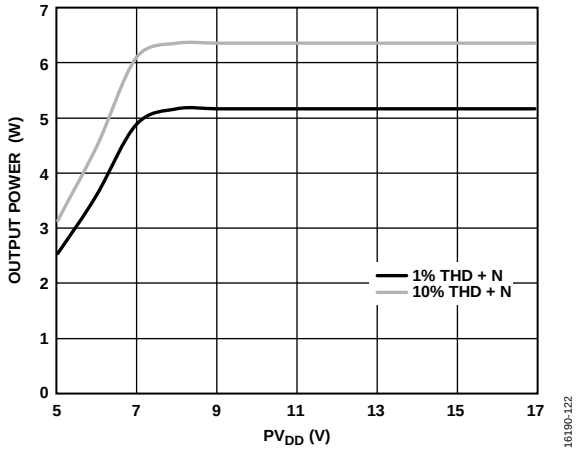

Figure 28. Output Power vs. PV_{DD}, R_L = 4 Ω, Analog Gain = 6.3

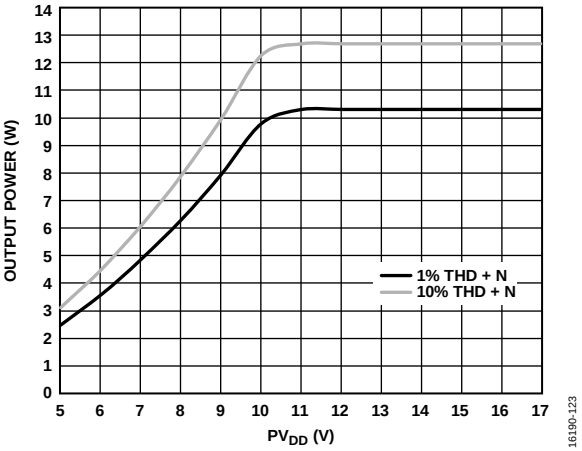

Figure 29. Output Power vs. PV_{DD} Supply Voltage, R_L = 4Ω, Analog Gain = 8.9

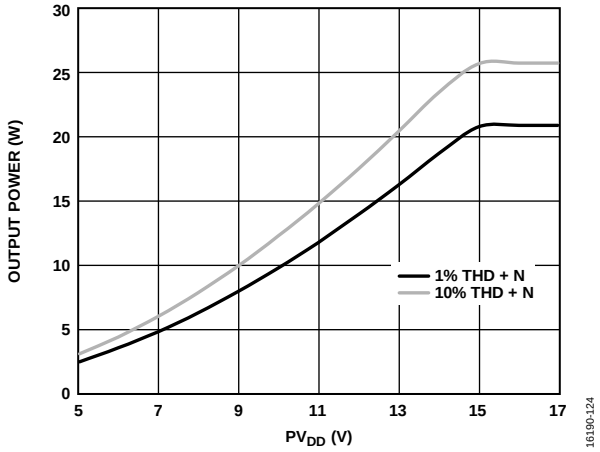

Figure 30. Output Power vs. PV_{DD}, R_L = 4 Ω, Analog Gain = 12.6

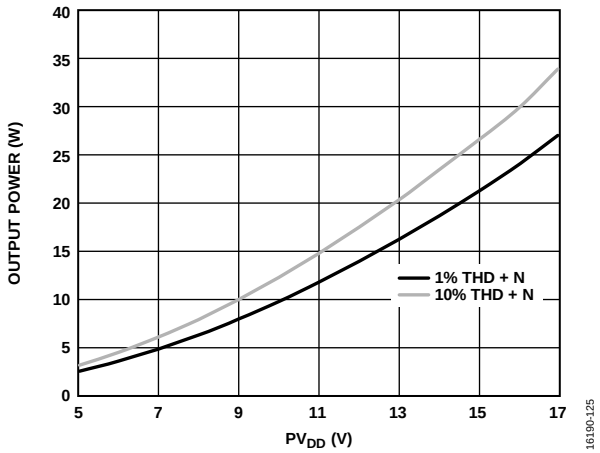

Figure 31. Output Power vs. PV_{DD}, R_L = 4 Ω, Analog Gain = 16

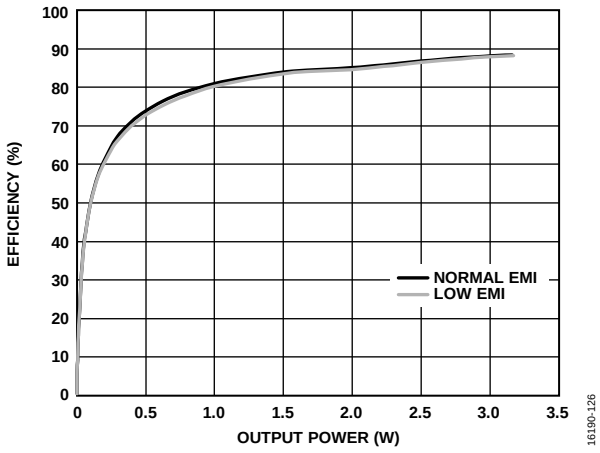

Figure 32. Efficiency vs. Output Power (P_{OUT}), R_L = 4 Ω, No Ferrite Bead (FB) and 220 pF Capacitor, PV_{DD} = 5 V, Analog Gain = 6.3

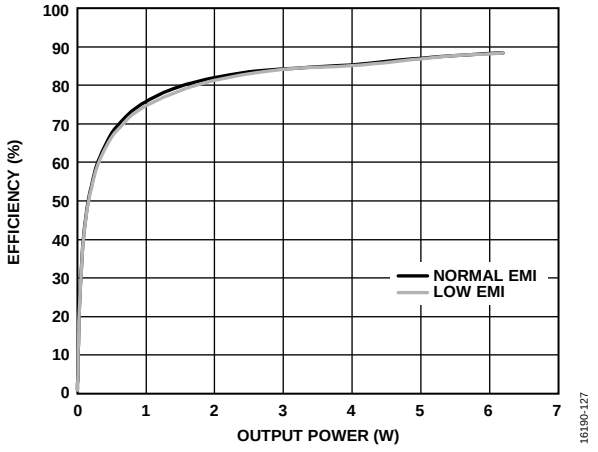

Figure 33. Efficiency vs. Output Power (P_{OUT}), R_L = 4 Ω, No Ferrite Bead (FB) and 220pF Capacitor, PV_{DD} = 7 V, Analog Gain = 8.9

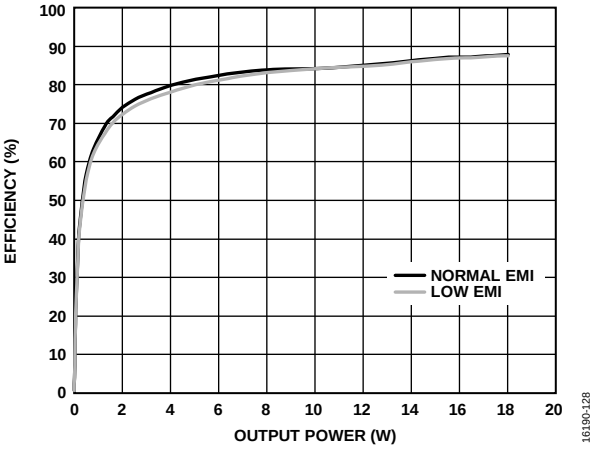

Figure 34. Efficiency vs. Output Power (P_{OUT}), R_L = 4 Ω, No Ferrite Bead (FB) and 220 pF Capacitor, PV_{DD} = 12 V, Analog Gain = 12.6

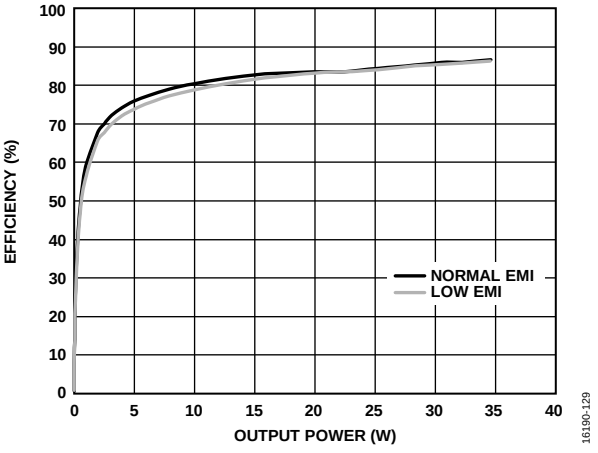

Figure 35. Efficiency vs. Output Power (P_{OUT}), R_L = 4 Ω, No Ferrite Bead (FB) and 220 pF Capacitor, PV_{DD} = 17 V, Analog Gain = 16

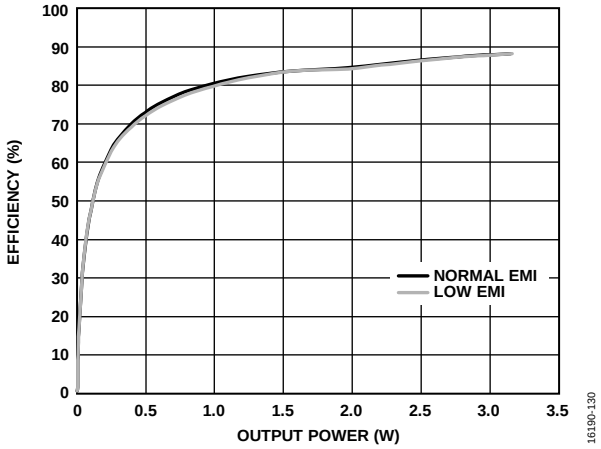

Figure 36. Efficiency vs. Output Power (P_{OUT}), R_L = 4 Ω, FB and 220 pF Capacitor, PV_{DD} = 5 V, Analog Gain = 6.3

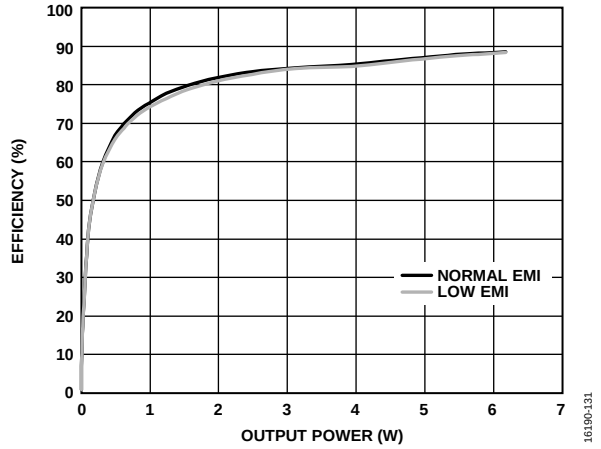

Figure 37. Efficiency vs. Output Power (P_{OUT}), R_L = 4 Ω, FB and 220 pF Capacitor, PVDD = 7 V, Analog Gain = 8.9

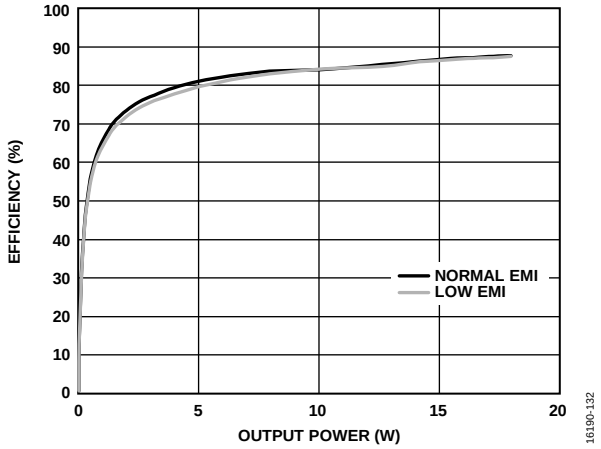

Figure 38. Efficiency vs. Output Power (P_{OUT}), R_L = 4 Ω, FB and 220 pF Capacitor, PV_{DD} = 12 V, Analog Gain = 12

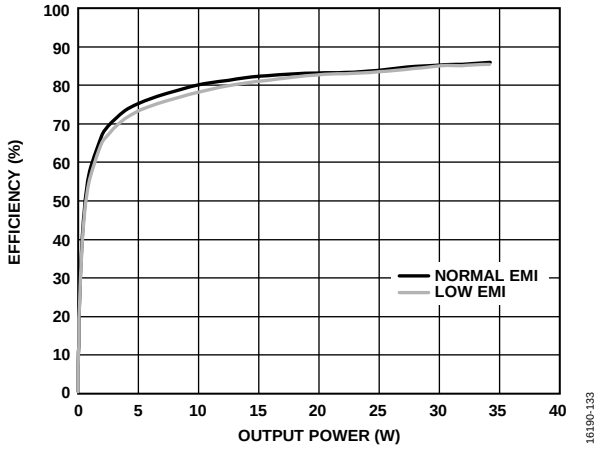

Figure 39. Efficiency vs. Output Power (P_{OUT}), R_L = 4 Ω, FB and 220 pF Capacitor, PV_{DD} = 17 V, Analog Gain = 16

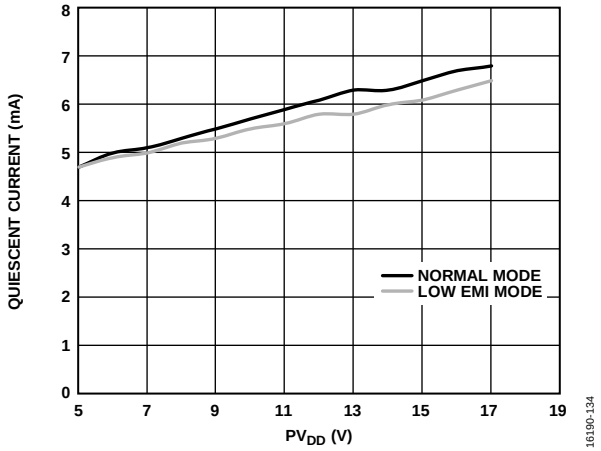

Figure 40. Quiescent Current, R_L = 4 Ω, No FB and 220 pF Capacitor, Analog Gain = 12.6

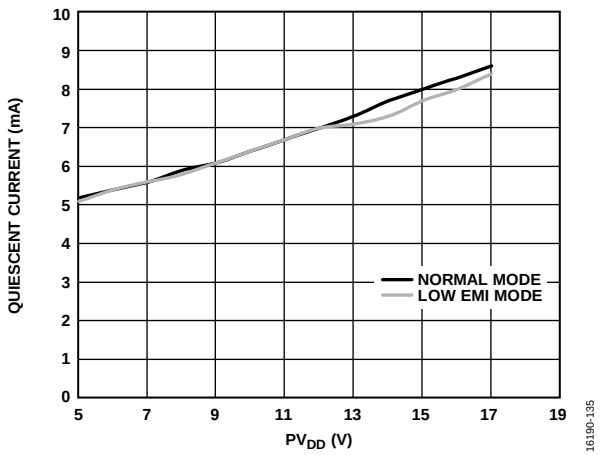

Figure 41. Quiescent Current, R_L = 4 Ω, FB and 220 pF Capacitor, Analog Gain = 12.6

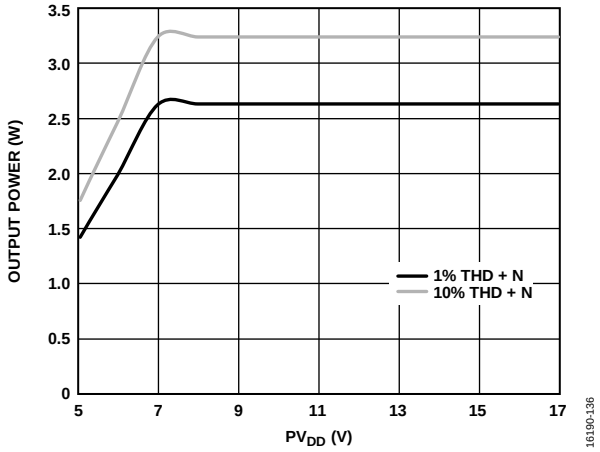

Figure 42. Output Power vs. PV_{DD} Supply Voltage (PV_{DD}), R_L = 8 Ω, Analog Gain = 6.3

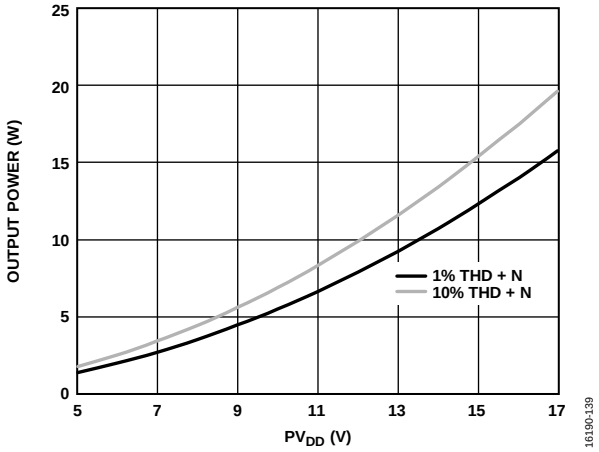

Figure 45. Output Power vs. PV_{DD} Supply Voltage (PV_{DD}), R_L = 8 Ω, Analog Gain = 16

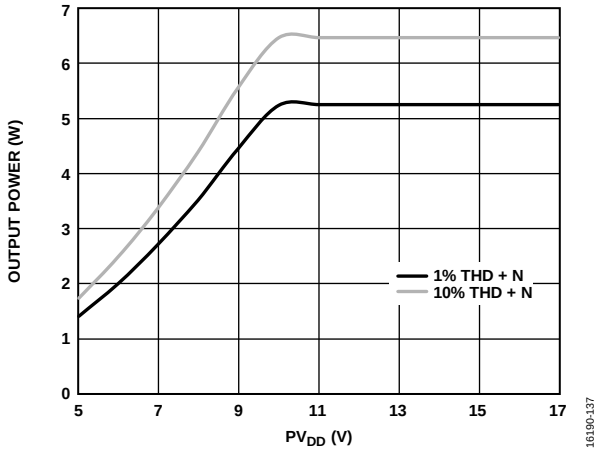

Figure 43. Output Power vs. PV_{DD} Supply Voltage (PV_{DD}), R_L = 8 Ω, Analog Gain = 8.9

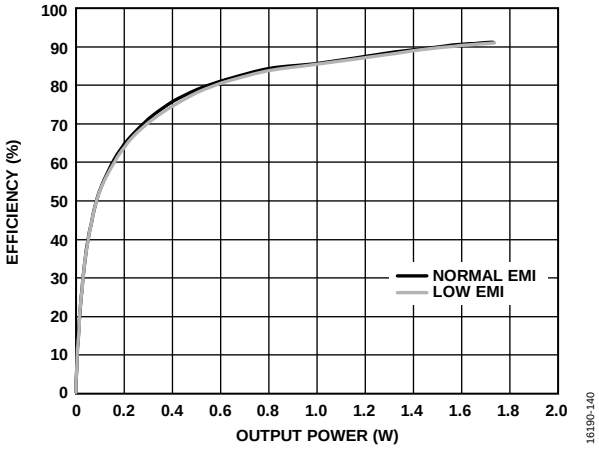

Figure 46. Efficiency vs. Output Power (P_{OUT}), R_L = 8 Ω, No FB and 220 pF Capacitor, PV_{DD} = 5 V, Analog Gain = 6.3

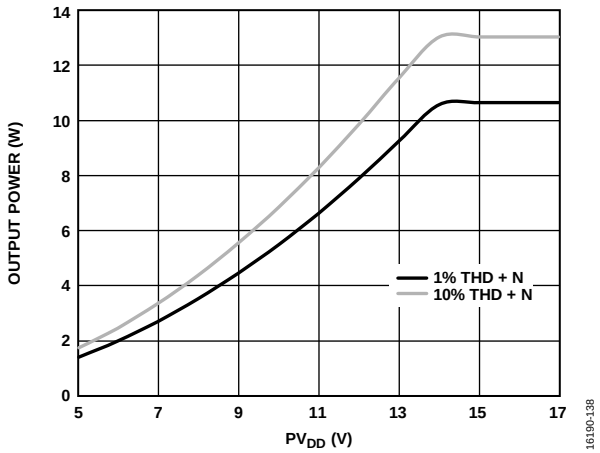

Figure 44. Output Power vs. PV_{DD} Supply Voltage (PV_{DD}), R_L = 8 Ω, Analog Gain = 12.6

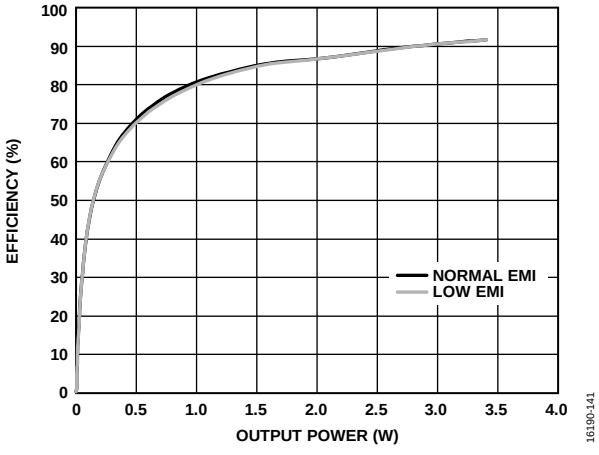

Figure 47. Efficiency vs. Output Power (P_{OUT}), R_L = 8 Ω, No FB and 220 pF Capacitor, PV_{DD} = 7 V, Analog Gain = 8.9

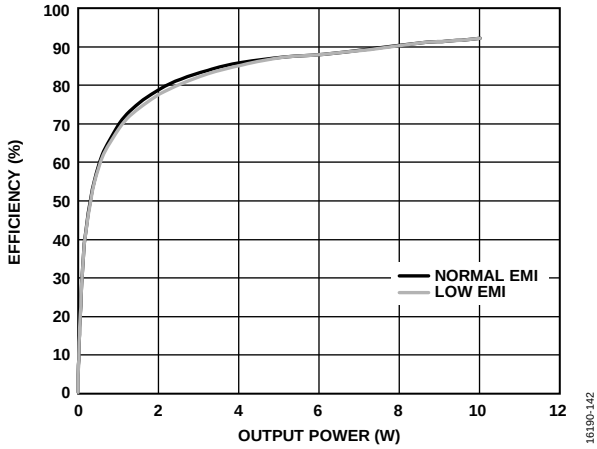

Figure 48. Efficiency vs. Output Power (P_{OUT}), R_L = 8 Ω, No FB and 220 pF Capacitor, PV_{DD} = 12 V, Analog Gain = 12.6

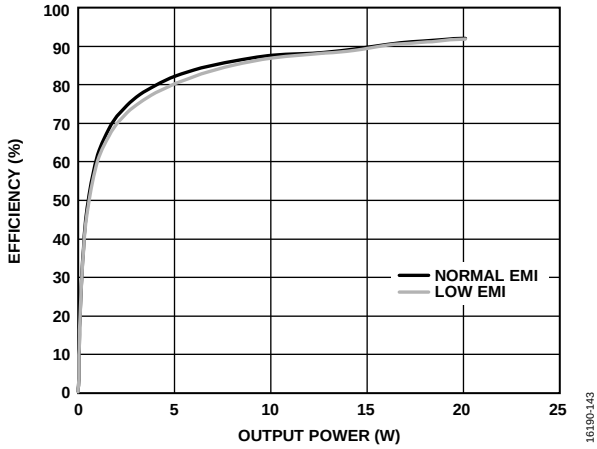

Figure 49. Efficiency vs. Output Power (P_{OUT}), R_L = 8 Ω, No FB and 220 pF Capacitor, PV_{DD} = 17 V, Analog Gain = 16

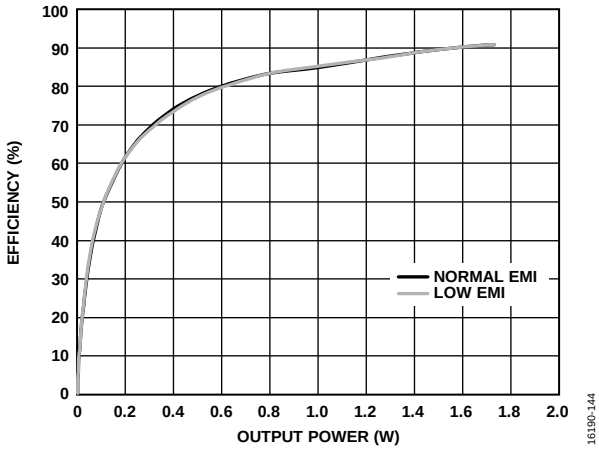

Figure 50. Efficiency vs. Output Power (P_{OUT}), R_L = 8 Ω, FB and 220 pF Capacitor, PV_{DD} = 5 V, Analog Gain = 6.3

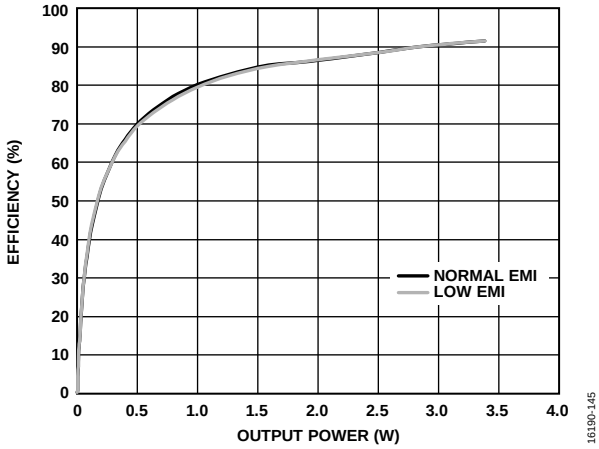

Figure 51. Efficiency vs. Output Power (P_{OUT}), R_L = 8 Ω, FB and 220 pF Capacitor, PV_{DD} = 7 V, Analog Gain = 8.9

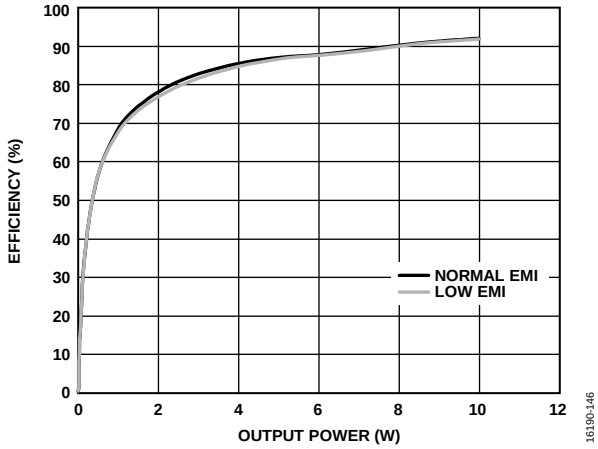

Figure 52. Efficiency vs. Output Power (P_{OUT}), R_L = 8 Ω, FB and 220 pF Capacitor, PV_{DD} = 12 V, Analog Gain = 12.6

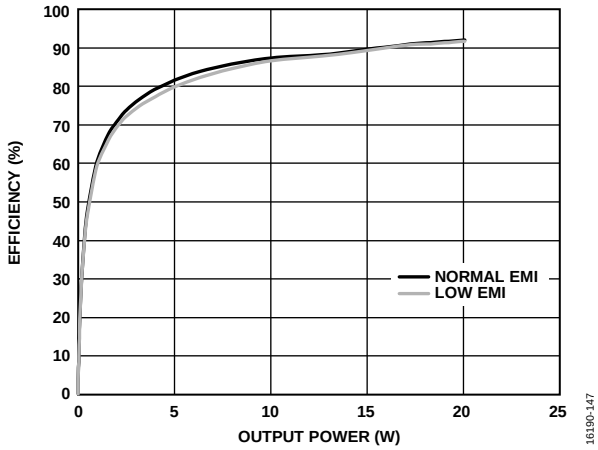

Figure 53. Efficiency vs. Output Power (P_{OUT}), R_L = 8 Ω, FB and 220 pF Capacitor, PV_{DD} = 17 V, Analog Gain = 16

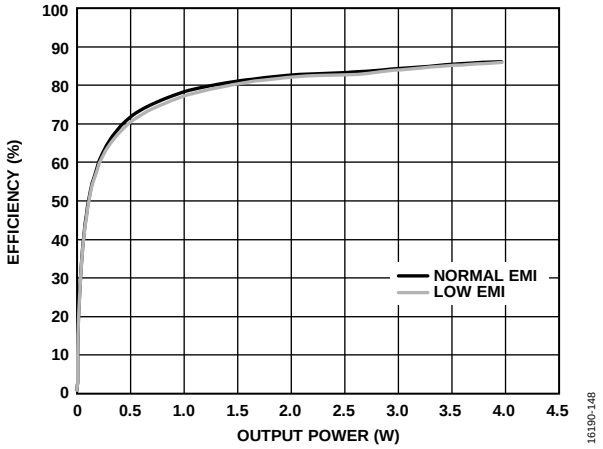

Figure 54. Efficiency vs. Output Power (P_{OUT}), R_L = 3 Ω, No FB and 220 pF Capacitor, PV_{DD} = 5 V, Analog Gain = 6.3

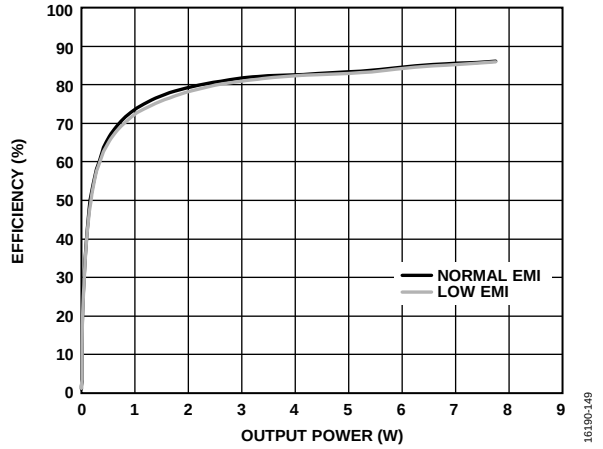

Figure. Efficiency vs. Output Power (P_{OUT}), R_L = 3 Ω, No FB and 220 pF Capacitor, PV_{DD} = 7 V, Analog Gain = 8.9

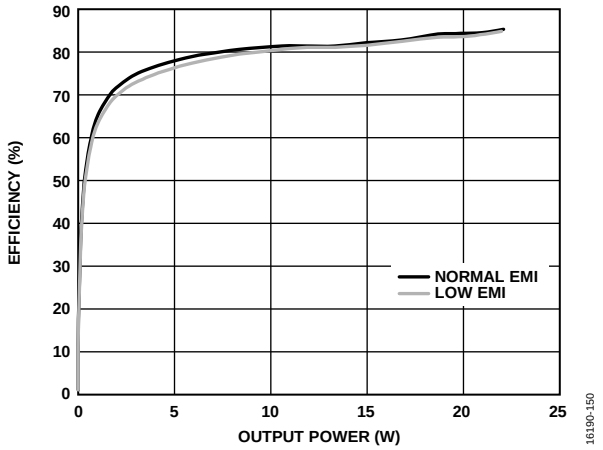

Figure 55. Efficiency vs. Output Power (P_{OUT}), RL = 3 Ω, No FB and 220 pF Capacitor, PV_{DD} = 12 V, Analog Gain = 12.6

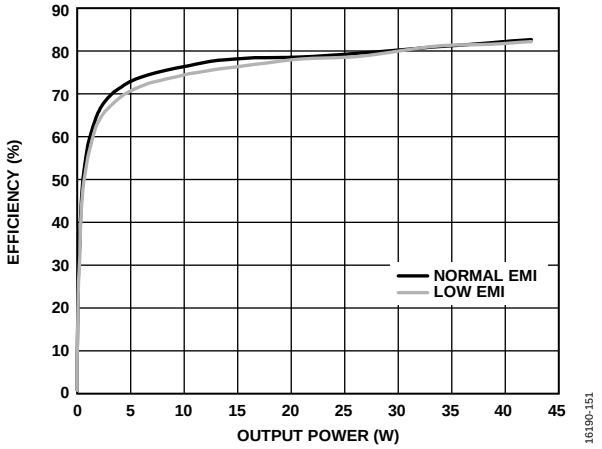

Figure 56. Efficiency vs. Output Power (P_{OUT}), R_L = 3 Ω, No FB and 220 pF Capacitor, PV_{DD} = 17 V, Analog Gain = 16

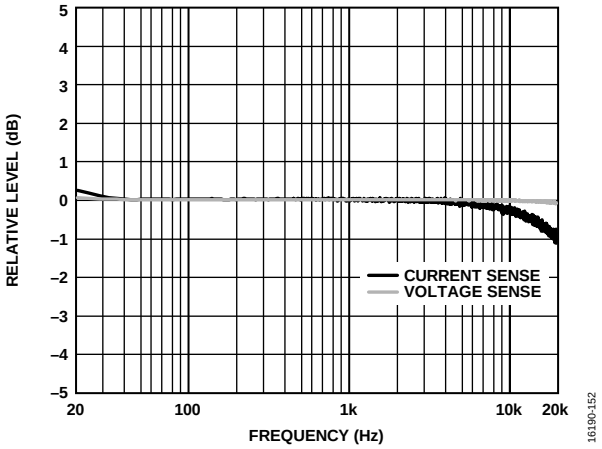

Figure 57. Current Voltage (I/V) Sense Frequency Response, −20 dBFS Input Signal, PV_{DD} = 12 V, Analog Gain = 12.6

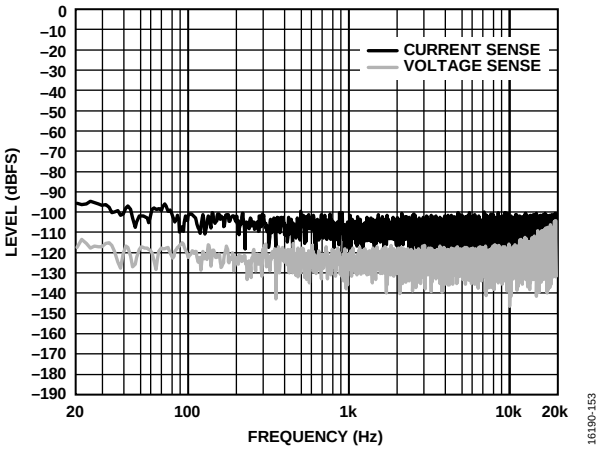

Figure 58. I/V Sense FFT, No Signal, PV_{DD} = 12 V, Analog Gain = 12.6

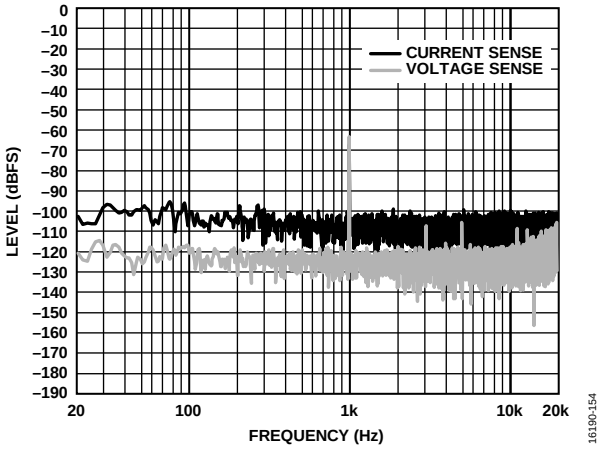

Figure 59. I/V Sense Output FFT, −60 dBFS Input, PV_{DD} = 12 V, Analog Gain = 12.6

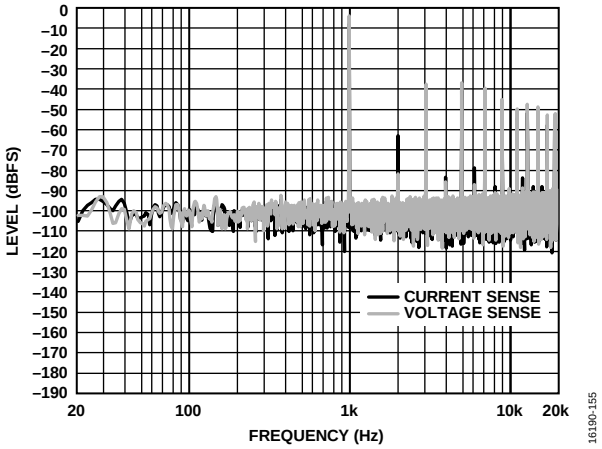

Figure 60. I/V Sense Output FFT, −1 dBFS Input, PV_{DD} = 12 V, Analog Gain = 12.6

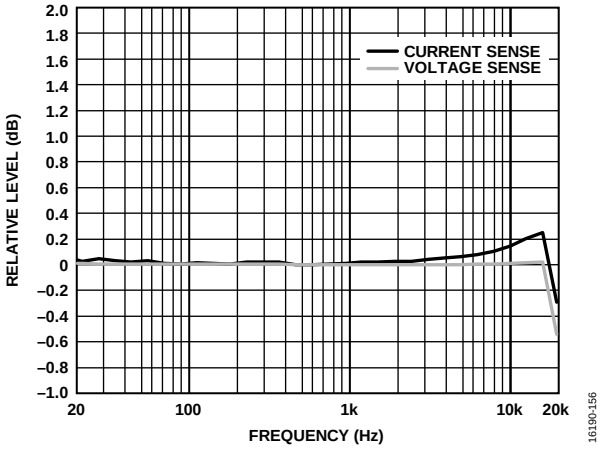

Figure 61. I/V Sense Linearity, −20 dBFS Input, PV_{DD} = 12 V, Analog Gain = 12.6

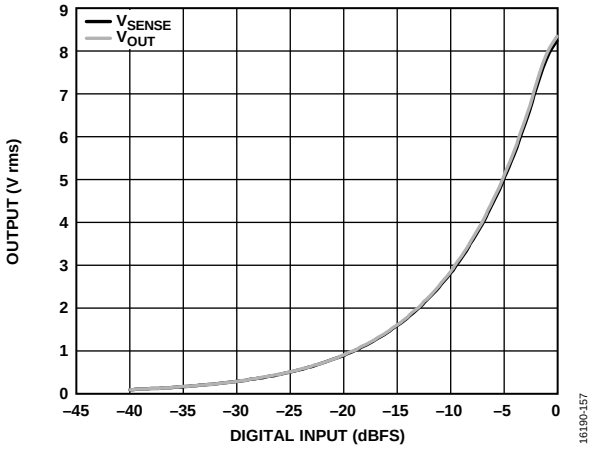

Figure 62. Voltage Sense Output vs. Amplifier Output V_{RMS}, PV_{DD} = 12 V, Analog Gain = 12.6

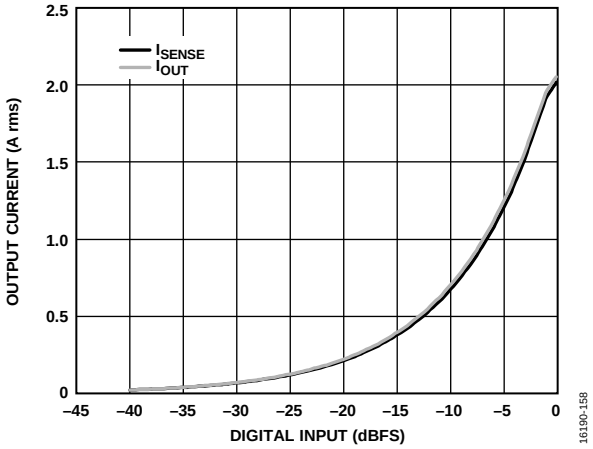

Figure 63. Current Sense Output vs. Amplifier Output Current Arms, PV_{DD} = 12 V, Analog Gain = 12.6

TYPICAL APPLICATION CIRCUITS

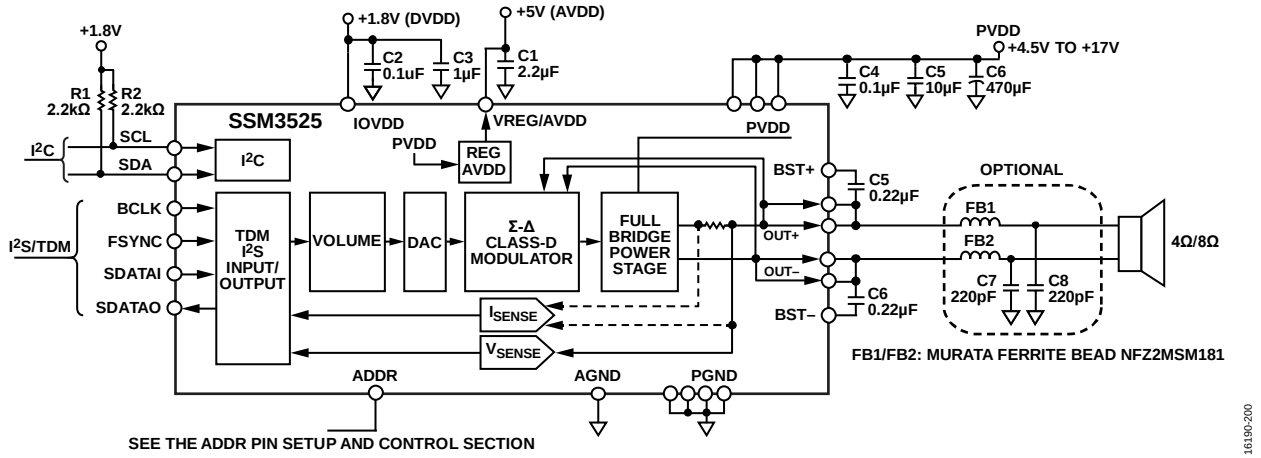

Figure 64. Typical Application Circuit

THEORY OF OPERATION

OVERVIEW

The SSM3525 Class D audio amplifier features a filterless modulation scheme that reduces the external component count, conserving board space and reducing system cost. The SSM3525 does not require an output filter; it relies on the inherent inductance of the speaker coil and the natural filtering of the speaker and human ear to recover the audio component of the square wave output. Most Class D amplifiers use some variation of pulse-width modulation (PWM), but the SSM3525 uses sigma-delta (Σ-Δ) modulation to determine the switching pattern of the output devices, resulting in a number of important benefits: Σ-Δ modulators do not produce a sharp peak with many harmonics in the amplitude modulation (AM) broadcast band, as PWMs often do. Σ-Δ modulation reduces the amplitude of spectral components at high frequencies, reducing EMI emission that can otherwise be radiated by speakers and long cable traces. Due to the inherent spread spectrum nature of Σ-Δ modulation, the need for oscillator synchronization is eliminated for designs incorporating multiple SSM3525 amplifiers.

The SSM3525 also integrates overcurrent and temperature protection and a thermal warning with optional programmable gain reduction.

The SSM3525 contains output voltage and current sensing with digitization. It also has a temperature sensor and a supply voltage sensor for the PVDD pin. The PVDD pin is typically connected to the battery or power supply in the system.

The SSM3525 supports two main modes of operation with control and data supplied through the I²C and TDM/I²S ports (see Table 12).

POWER SUPPLIES

The power supply pins on the SSM3525 are as follows:

- PVDD, the power supply, is used for the output stage.
- AV_{DD} is the analog supply used for the input stage, modulator, power stage gate drive, and other blocks. It can be generated internally by the integrated linear regulator. Alternatively, if higher system efficiency is needed, connect the AVDD pin to an external 5 V supply in the system.
- If the REG_EN control register is set to 1, the internal regulator is enabled; otherwise, an external 5 V supply is required.
- I_{OVDD} is the digital supply voltage for the serial audio interface and internal digital circuitry. It must be supplied externally.

ADDR PIN SETUP AND CONTROL

The SSM3525 supports I²C control. The ADDR pin can be set to four different levels: pulled to GND, pulled up to IOV_{DD} via a 47 kΩ resistor, pulled down to ground via a 47 kΩ resistor, or left open. The state of the ADDR pin determines the I²C device address. By default in I²C mode, the device uses the BCLK, FSYNC, SDATAI, and SDATAO pins for TDM/I²S data. Alternatively, the device can be set to receive and transmit PDM data by setting the PDM_MODE register bit field. See Table 12 for setting up the desired mode.

Table 11. I²C Address Selection

ADDR Pin Connection	Control Port Mode	IOV_{DD} Range (V)	I²C Address
GND	I²C	1.2 to 1.8	0x24
Pull Down	I²C	1.2 to 1.8	0x25
Open	I²C	1.2 to 1.8	0x26
Pull Up	I²C	1.2 to 1.8	0x27
IOVDD	Reserved	Not applicable	Not applicable

Table 12. Serial Port Mode Setup for I²S, TDM, and PDM

Serial Port Mode	IOV_{DD} Range	Description	Pin Usage			
			BCLK Pin	SDATAO Pin	FSYNC Pin	SDATAI Pin
I²S/TDM	1.2 V to 1.8 V	Sets the part into default I²S/TDM mode	Bit clock input	Sense data output I²S/TDM format	Frame clock input	Data input I²S/TDM format
PDM	1.2 V to 1.8 V	Set the PDM_MODE bit to 1 in Register 0x21, use FSYNC pin for setting the left/right channel	PDM clock input	Sense data output PDM format	GND (left channel) and IOVDD (right channel)	Data input PDM format

POWER-DOWN MODES

The SSM3525 can be powered down by several methods. Setting the SPWDN bit to 1 in Register 0x20 fully powers down the device except for the I²C interface. Individual blocks can also be powered on or off via the block level power-down controls.

For lowest power shutdown, the SSM3525 also contains a clock loss detection circuit that monitors the BCLK input clock. When no BCLK is present, the device automatically powers down all internal circuitry to its lowest power state. When BCLK returns, the device automatically powers up following its usual power sequence.

There is an optional auto power-down feature when using I²S/TDM: the device enters a lower power state when 2048 consecutive zero input samples are received. The device automatically powers back up from this state once a single nonzero value sample is received. Only the I²C and digital audio input blocks are active.

OUTPUT CURRENT SENSING

The SSM3525 uses an integrated sense resistor (50 mΩ typical) to determine the output current flowing to the load. The voltage across this sense resistor is proportional to the load current and sent to a 1-bit ADC running nominally at 128 × fs. The sense voltage can be output in I²S/TDM format in I²S/TDM mode or via the PDM interface in PDM mode. The output of this ADC can also be downsampled using digital filtering. The data is 16 bits, twos complement and in signed fraction format. This downsampled signal is at an 8 kHz to 192 kHz sample rate. It can be output on the SDATAO pin.

To set a different sample rate for both current and voltage sensing, use the SNS_FS bit in Register 0x05.

OUTPUT VOLTAGE SENSING

The output voltage level is monitored at the OUT± pins and sent to a 1-bit analog to digital converter running nominally at 128 × fs. This can be output in PDM format in PDM mode or via the PDM interface in PDM mode. The output of this ADC is can also be downsampled using digital filtering. This downsampled signal at 8 kHz to 192 kHz sample rate is output on the digital audio interface. The data is 16 bits twos complement and in signed fraction format. It can be output on the SDATAO pin.

TEMPERATURE SENSOR

The SSM3525 contains an 8-bit ADC that measures the die temperature of the device and is enabled via the TEMP_PWDN bit in Register 0x20. After the sensor is enabled, the temperature sense value can be read via the I²C in Register 0x12 in an 8-bit, unsigned format.

The ADC input range is fixed internally from −60°C to +195°C. To convert the hexadecimal value to the temperature (Celsius) value, use the following steps:

1. Convert the hexadecimal value to decimal and then subtract 60. For example, if the hexadecimal value is 0x54, the decimal value is 84.
2. Calculate the temperature using the following equation:

$$Temperature = Decimal\ Value - 60$$

3. With a decimal value of 84, *Temperature* = 84 − 60 = 24°C

PCM DIGITAL AUDIO SERIAL INTERFACE

The SSM3525 includes a standard serial audio interface that is slave only and used when in I²C mode. The interface is capable of receiving and transmitting I²S, left justified, pulse code modulated (PCM), or TDM formatted data.

There is an input interface for sending audio to the DAC and amplifier and an output interface for the sense, temperature, and automatic gain control (AGC) gain data. These interfaces share the same FSYNC and BCLK signals.

Provide a BCLK signal to the SSM3525 for correct operation. The BCLK signal must have a minimum frequency of 2.048 MHz. The BCLK signal internally clocks the device. The BCLK rate is auto detected, but the sampling frequency must be known to the device. At the 32 kHz to 48 kHz sample rate, the supported BCLK rates are 50, 64, 100, 128, 150, 192, 200, 250, 256, 384, 400, 500, 512, 768, 800, and 1024 times the sample rate.

The serial interfaces have three main operating modes. Stereo modes, typically I²S or left justified, are used when there are one or two chips on the interface bus. TDM modes are more flexible and can support up to 32 chips on the bus. These mode selections can be set via the I²C interface with the SAI_MODE bit.

The SAI_DRV bit setting determines the state of the SDATAO pin during the unused bit clock cycles. When the SAI_DRV bit is set to 1, the SDATAO pin is driven to logic low or not driven (high-Z) when set to 0. If using multiple chips on the serial interface bus, SAI_DRV bit must be set to 0.

STEREO (I²S/LEFT JUSTIFIED) OPERATING MODE

Stereo modes use both edges of the FSYNC signal to determine placement of data. Stereo mode is enabled when SAI_MODE = 0 and the I²S or left justified format is determined by the SDATA_FMT bit.

The I²S or left justified formats accepts any number of BCLK cycles per FSYNC cycle.

The six placement control registers (Address 0x24 to Address 0x29) determine placement of input and output data. Odd numbered placement control registers determine the order on the left channel and even number on the right channel.

Sample rates from 8 kHz to 192 kHz are accepted.

TDM OPERATING MODE

The TDM operating mode allows multiple chips to use a single serial interface bus.

The FSYNC signal operates at the desired sample rate. A rising edge of the FSYNC signal indicates the start of a new frame. For proper operation, this signal must be one BCLK cycle wide, transitioning on a falling BCLK edge. The MSB of the data presents on the SDATAO signal one BCLK cycle later. The SDATAO signal must be latched on a rising edge of BCLK.

Each chip on the TDM bus can occupy 16, 24, 32, 48, or 64 BCLK cycles. This is set with the TDM_BCLKS bit in Register 0x22 and all chips on the bus must have the same setting. Up to 32 SSM3525 chips can be used on a single TDM bus, but only four unique I²C device addresses are available. The SSM3525 automatically determines how many possible chips can be placed on the bus from the BCLK rate. There is no limit to the total number of BCLK cycles per FSYNC pulse, except for the maximum 50 MHz frequency of BCLK.

The chip slot of multiple SSM3525 devices used are determined by the TDM_SLOT bits.

The six placement control registers determine placement of input and output data within each chip slot. For input data to the DAC, either 16-bit or 24-bit data can be selected. For output data, there are multiple options available for placing the voltage sense, current sense, temperature sense, and P_{VDD} voltage information. See Bits Px_SNS in Register 0x24 to Register 0x29.

SERIAL DATA PLACEMENT

The SSM3525 is flexible in where within a frame it places output data and where it looks for input data. There are four control bits (Px_DAC) for when input data is expected and six control bits (Px_SNS) for when output data is driven.

A single data frame is broken up into individual fields, referred to as placements. Each placement can be 8 bits, 16 bits, or 24 bits in length. A single frame on the TDM or I²S data stream can contain several data placements of varying length.

When the serial port is operating in TDM mode, placements start directly after the FSYNC pulse. The first placement is referred to as P1, and the second placement is referred to as P2, for example, increasing sequentially. These placements appear in sequential order on the serial data signal.

Up to four placements can be on the input stream and up to six placements can be on the output stream. Figure 65 shows a basic timing diagram of the placements in TDM mode.

When the serial port is operating in I²S mode, placements start directly after the FSYNC falling clock edge, signaling the beginning of a new frame. The first placement is referred to as P1, the second placement is referred to as P2, for example, increasing sequentially. The odd numbered placements (P1, P3, and P5) appear sequentially in the left channel, when the FSYNC signal is low (assuming FSYNC_MODE = 0), and the even numbered placements (P2, P4, and P6) appear sequentially in the right channel, when the FSYNC signal is high (assuming FSYNC_MODE = 0). Up to four placements can be on the input stream and up to six placements can be on the output stream. Figure 66 shows a basic timing diagram of the placements in I²S mode.

The corresponding registers (Address 0x22 to Address 0x29) allow configuration of each data placement. An input placement (Px_DAC) can carry 24-bit audio data, 16-bit audio data, or 8 zero bits that are used as padding and ignored. A sense placement (Px_SNS) can contain 16-bit voltage output data, 16-bit current output data, 8-bit battery voltage data, 8-bit temperature data, alternating 16-bit voltage and current data, 8-bit status data, 8-bit V/I marker and status data, or 8 zero bits.

For standard I²S mode, the serial input is configured to receive mono audio data and the serial output is configured to send voltage, current, and battery data back to the host device. The default register settings correspond to the timing diagram in Figure 67.

When the 8-bit status output is selected, that 8-bit placement area outputs the same bits that are found in the read only STATUS register. The format can be seen in Table 13. When the 8-bit V/I marker and status output placement is selected, the MSB indicates whether voltage sense or current sense is being output on that sample frame, and the 7 LSBs correspond to the STATUS register, the formatting for can be seen in Figure 14.

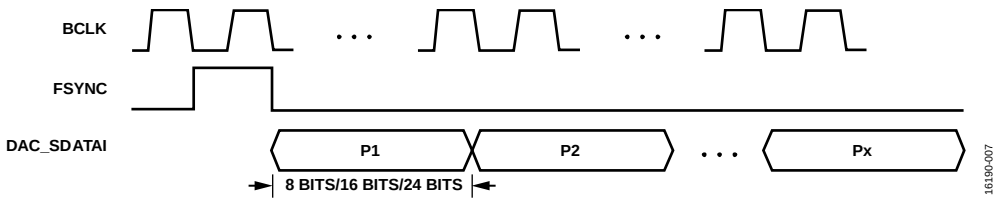

Figure 65. Basic Timing Diagram of Placements in TDM Stream

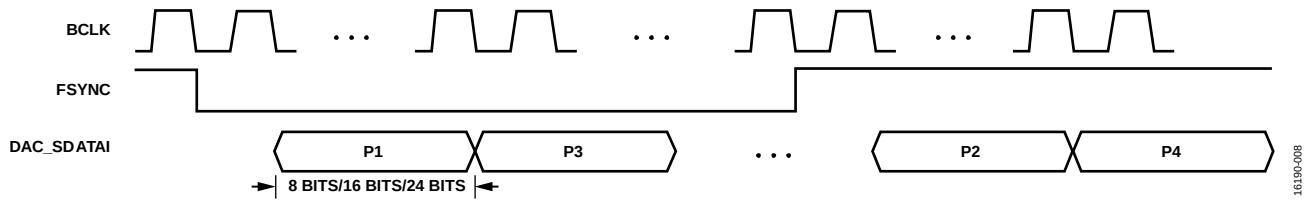

Figure 66. Basic Timing Diagram of Placements in I²S Stream

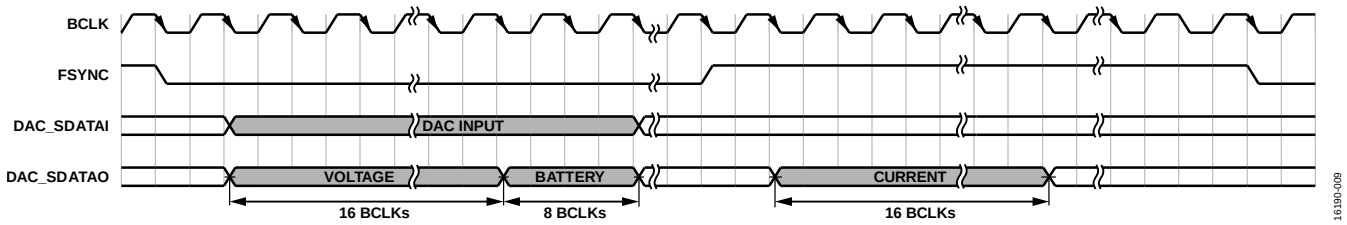

Figure 67. Standard I²S Data Placement Timing Diagram

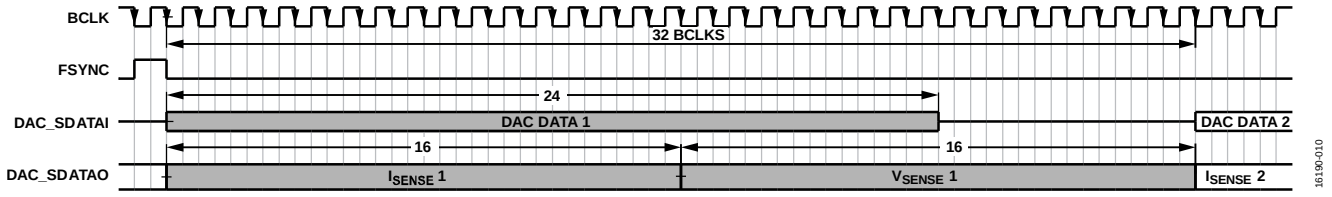

Figure 68. TDM Serial Interface Format

Table 13. 8-Bit Status Sense Output Format (STATUS Register)

Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
UVLO_VREG	UVLO_PVDD	LIM_EG	CLIP	AMP_OC	OTF	OTW	BAT_WARN

Table 14. 8-Bit V/I Marker and Status Sense Output Format (STATUS Register)

Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
1 = VSENSE, 0 = ISENSE	UVLO_PVDD	LIM_EG	CLIP	AMP_OC	OTF	OTW	BAT_WARN

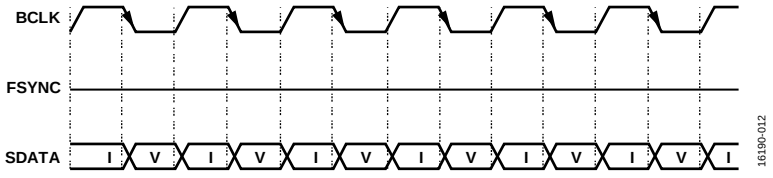

Figure 69. SDATA Output in PDM Mode

PDM OPERATING MODE

By setting the PDM_MODE bit in Register 0x21 to 1, the 1-bit PDM data from the sense ADCs can be output directly on SDATAO, and the DAC can be driven with 1-bit PDM data on SDATAI. In this case, a 2.048 MHz to 6.144MHz CLK must be provided on the BCLK pin.

PDM input data is latched on both edges of the clock. The FSYNC pin state determines which channel (left or right) is sent to the DAC.

Table 15. FSYNC Settings for PDM Mode

SDATA Input	FSYNC Pin Configuration
Use L Channel Data	Connect to IOVDD
Use R Channel Data	Connect to GND

PDM data is output on both edges of the clock. The current sense ADC data is output when BCLK is high, and the voltage sense ADC data is output when BCLK is low. Refer to Table 12 and Figure 69.

ANALOG AND DIGITAL GAIN

There are several selectable settings for the analog gain of the system via the ANA_GAIN bits. These bits are designed to provide optimal gain staging at various PV_{DD} supply voltages.

There is also a digital gain/volume control in the DAC_VOL register that provides fine control in 0.375 dB steps from −70 dB to +24 dB.

PV_{DD} (V_{BAT}) SENSING

The SSM3525 contains an 8-bit ADC that measures the voltage of the battery voltage (V_{BAT}) supply. The battery voltage information is stored in Register 0x13 as an 8-bit unsigned format. The ADC input range is fixed internally as 4 V to 18 V. To convert the hexidecimal value to the voltage value, use the following steps:

1. Convert the hex value to decimal. For example, if the hexadecimal value is 0xA9, the decimal value is 169.
2. Calculate the voltage using the following equation:

$$Voltage = 4\ V + 14\ V \times Decimal\ Value/255$$

With a decimal value of 169,

$$Voltage = 4\ V + 14\ V \times 169/255 = 13.278\ V$$

This data can be output on the SDATAO pin along with V/I sense data or read via the V_{BAT} register over the control interface, as previously mentioned.

FAULTS AND LIMITER STATUS REPORTING

The SSM3525 offers comprehensive protections against the faults at the outputs and reporting to help with system design. The faults listed in Table 16 are reported using the status registers.

Table 16. Register 0x11 Faults

Fault Type	Flag Set Condition	Status Reported Register
5 V Regulator or AV_{DD} Undervoltage (UV)	5 V regulator voltage at VREG/ AV_{DD} < 3.6 V	Register 0x11, Bit 7, UVLO_VREG
PV_{DD} Undervoltage	When PV_{DD} < 3.6V	Register 0x11, Bit 6, UVLO_PVDD
Limiter/Gain Reduction Engage	Limiter engaged	Register 0x11, Bit 5, LIM_EG
Clipping	DAC clipping	Register 0x11, Bit 4, CLIP
Output Overcurrent (OC)	Output current > 6 A peak	Register 0x11, Bit 3, AMP_OC
Die Overtemperature (OT)	Die temperature > 145°C	Register 0x11, Bit 2, OTF
Die Overtemperature Warning (OTW)	Die temperature > 117°C	Register 0x11, Bit 4, OTW
Battery Voltage > VBAT_INF	Battery voltage PV_{DD} > VBAT_INF	Register 0x11, Bit 0, BAT_WARN

The faults listed in Table 16 are reported in Register 0x11 and can be read via I^2C by the microcontroller in the system.

In the event of a fault occurrence, how the device reacts to the faults can be controlled by using Register 0x10.

Table 17. Register 0x10 Fault Recovery

Fault Type	Flag Set Condition	Status Reported Register
OTW	The amount of gain reduction applied if there is an OTW	Register 0x10, Bits[7:6], OTW_GAIN
Manual Recovery	Use to attempt manual recovery in case of a fault event	Register 0x10, Bit 5, MRCV
Autorecovery Attempts	When autorecovery from faults is used, set the number of attempts using this bit	Register 0x10, Bits[4:3], MAX_AR
UV	Recovery can be automatic or manual	Register 0x10, Bit 2, ARCV_UV
Die OT	Recovery can be automatic or manual	Register 0x10, Bit 1, ARCV_OT
OC	Recovery can be automatic or manual	Register 0x10, Bit 0, ARCV_OC

When the automatic recovery mode is set, the device attempts to recover itself after the fault event and, in case the fault persists, the device sets the fault again. This process repeats until the fault is resolved.

When using the manual recovery mode, the device shuts down and the recovery must be attempted using the system microcontroller.

LIMITER AND BATTERY TRACKING THRESHOLD CONTROL

The SSM3525 contains an output limiter that can limit the peak output voltage of the amplifier. The limiter works on the rms and peak value of the signal. The limiter threshold, slope, attack rate, and release rate are programmable using Register 0x08, Register 0x09, and Register 0x0A. The limiter can be enabled or disabled using LIM_EN, Bits[1:0] in Register 0x08.

The threshold at which the output starts limiting is determined by the LIM_THRES register setting, in Register 0x09, Bits[7:3]. When the ouput signal level exceeds the set threshold level, the limiter activates and limits the signal level to the set limit. Below the set threshold, the output level is not affected. The limiter threshold can be set from 2 V_{PEAK} to 16 V_{PEAK}.

The limiter threshold can be set above the maximum output voltage of the amplifier. In this case, the limiter allows maximum peak output; the output can clip depending on the power supply voltage and not the limiter.

The limiter threshold can be set as fixed or to vary with the battery voltage via the VBAT_TRACK bit (Register 0x08, Bit 2). When set to fixed, the limiter threshold is fixed and does not vary with battery voltage. The threshold can be set from 2 V_{PEAK} to 16 V_{PEAK} using the LIM_THRES bit (see Figure 71).

When set to a variable threshold, the SSM3525 monitors the V_{BAT} supply and automatically adjusts the limiter threshold based on the V_{BAT} supply voltage.

The V_{BAT} supply voltage at which the limiter threshold level begins to decrease the output level is determined by the VBAT inflection point, the VBAT_INF bits (Register 0x0A, Bits[7:0]).

The VBAT_INF point is defined as the battery voltage at which the limiter either activates or deactivates depending on the LIM_EN mode (see Table 18). When the battery voltage is greater than VBAT_INF, the limiter is not active. When the battery voltage is less than VBAT_INF, the limiter is activated. The VBAT_INF bits can be set from 4 V to 18 V. The 8-bit value for the voltage can be calculated using the following equation:

$$Voltage = 4 + 14 \times Decimal\ Value/255$$

Convert the decimal value to an 8-bit hexadecimal value and use it to set the VBAT_INF bits.

The rate at which the limiter threshold is lowered relative to the amount of change in VBAT below the VBAT_INF point is determined by the slope bits (Register 0x09, Bits[1:0]).

The slope is the ratio of the limiter threshold reduction to the VBAT voltage reduction.

$$Slope = \Delta Limiter\ Threshold/\Delta VBAT$$

The slope ratio can be set from 1:1 to 4:1. This function is useful to prevent early shutdown under low battery conditions. As the V_{BAT} voltage falls, the limiter threshold is lowered. The limiter reduces the output level, therefore helping reduce the current drawn from the battery and preventing early shutdown due to low VBAT.

The limiter offers various active modes, which can be set using the LIM_EN bits (Register 0x08, Bits[1:0]) and the VBAT_TRACK bit, as shown in Table 18.

When LIM_EN = 01, the limiter is enabled. When LIM_EN = 10, the limiter mutes the output if VBAT falls below VBAT_INF. When LIM_EN = 11, the limiter engages only when the battery voltage is lower than VBAT_INF.

When VBAT is above VBAT_INF, no limiting occurs. There is hysteresis around VBAT_INF for the limiter disengaging.

The limiter, when active, reduces the gain of the amplifier. The rate of gain reduction or attack rate is determined by the LIM_ATR bits (Register 0x08, Bits[5:4]). Similarly, when the signal level drops below the limiter threshold, the gain is restored. The gain release rate is determined by the LIM_RRT bits (Register 0x08, Bits[7:6]).

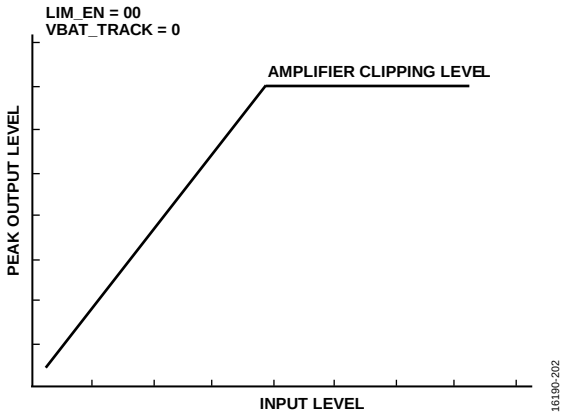

Figure 70. Limiter Example (LIM_EN = 0b00, VBAT_TRACK = 0bx)

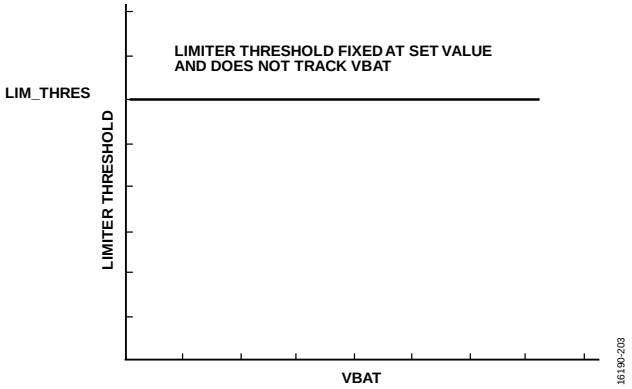

Figure 71. Limiter Fixed (LIM_EN = 0b01, VBAT_TRACK = 0b0)

Table 18. Limiter Modes

LIM_EN	VBAT_TRACK	Limiter	VBAT < VBAT_INF	VBAT > VBAT_INF	Comments
00	0 or 1	No	Not applicable	Not applicable	See Figure 70
01	0	Fixed	Use the set threshold	Use the set threshold	See Figure 71
01	1	Variable	Lowers the threshold	Use the set threshold	See Figure 72 and Figure 73
10	0 or 1	Fixed	Mutes the output	Use the set threshold	Not applicable
11	0	Fixed	Use the set threshold	No limiting	See Figure 74 and Figure 75
11	1	Variable	Lowers the threshold	No limiting	See Figure 76 and Figure 77

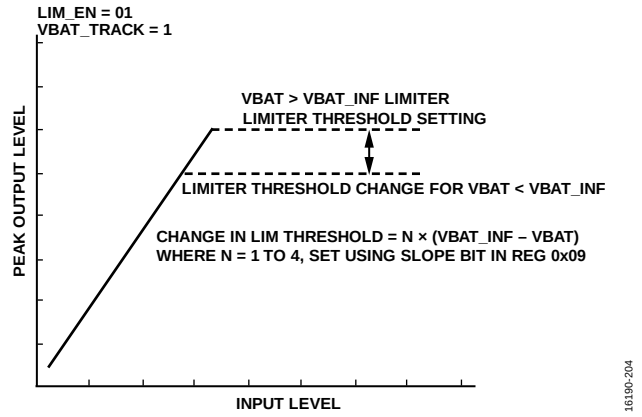

Figure 72. Limiter Fixed (LIM_EN = 0b01, VBAT_TRACK = 0b1)

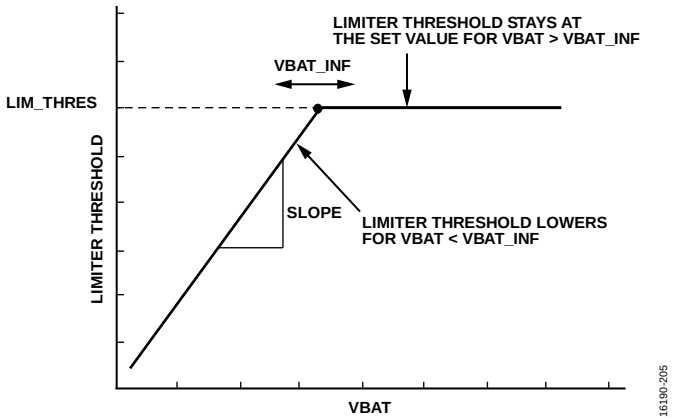

Figure 73. Output Level vs. VBAT in Limiter Tracking Mode (LIM_EN = 0b01, VBAT_TRACK = 0b1)

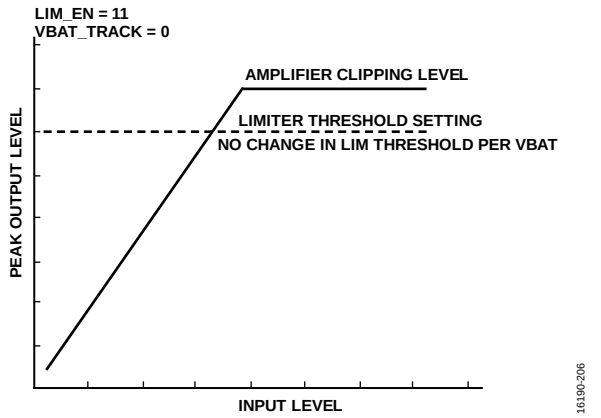

Figure 74. Limiter Example (LIM_EN = 0b11, VBAT_TRACK = 0)

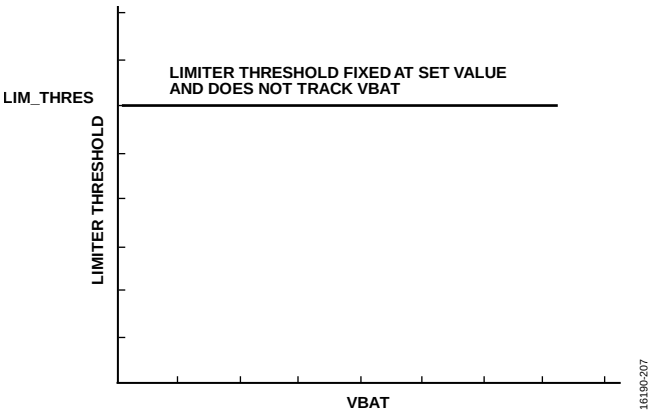

Figure 75. Limiter Fixed (LIM_EN = 0b11, VBAT_TRACK = 0b0)

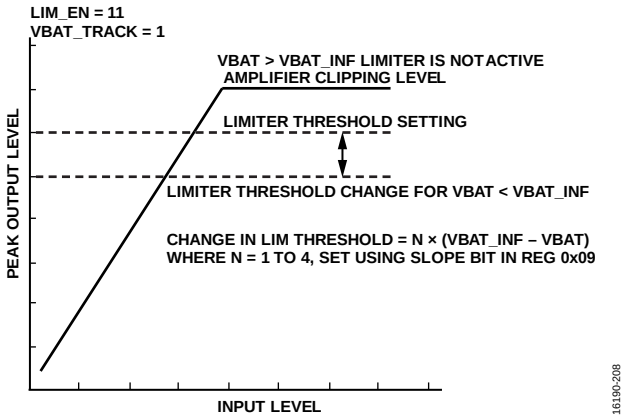

Figure 76. Limiter Example (LIM_EN = 0b11, VBAT_TRACK = 0b1)

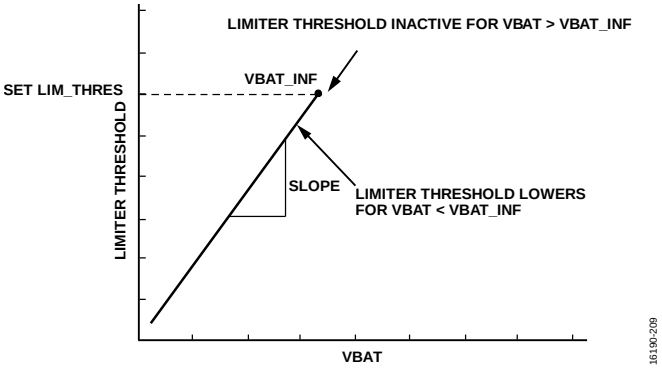

Figure 77. Output Level vs. VBAT in Limiter Tracking Mode (LIM_EN = 0b11, VBAT_TRACK = 0b1)

Linking Limiters of Multiple SSM3525 Devices

If multiple SSM3525 devices are used in a system, the gain adjustment from the limiters of all or some of the devices can be linked. The device internally generates the gain adjustment value (AGC_GAIN) based on the limiter settings. When limiters of multiple devices on the bus are linked, the device uses the highest (most gain reduction) gain adjustment value (AGC_GAIN) of all devices. Up to four SSM3525 devices can be linked in this manner.

To link the AGC_GAIN to other chips, the LIM_LINKx bits must be set in the LIM_LINK register, 0x0E.

When using I^2S/TDM, for every chip that is linked, the placement of its respective AGC_GAIN value within the TDM stream must be given. The AGC_GAIN data for a respective device is made available at the assigned slot using the AGC_GAINx_SLOT bits. The AGC_GAIN data is eight bits wide and in an assigned slot, these bits can be placed in any one of eight places in a 64-bit frame. This setting is available in the AGC_GAINx_PLACE register. These values can be set in Register 0x2A through Register 0x2D.

The audio signal is not affected by the AGC function unless the peak audio output voltage exceeds the limiter threshold level.

POP AND CLICK SUPPRESSION

Voltage transients at the output of audio amplifiers can occur when shutdown is activated or deactivated. Voltage transients as small as 10 mV can be heard as an audible pop in a speaker. Clicks and pops are defined as undesirable audible transients, generated by the amplifier system, that do not come from the system input signal.

Such transients can be generated when the amplifier system changes its operating mode. For example, system power-up and power-down can be sources of audible transients.

The SSM3525 has a pop and click suppression architecture that reduces these output transients, resulting in noiseless activation and deactivation.

Set either mute or power-down before the BCLK signal is removed to ensure a pop free power-down.

HIGH FREQUENCY CLIPPER

The high frequency clipper can be controlled via the DAC_CLIP bits (Register 0x0F, Bits[7:0]).

These bits determine the clipper threshold, relative to full scale. When enabled, the clipper digitally clips the signal after the DAC interpolation.

EMI NOISE

The SSM3525 uses a proprietary modulation and spread spectrum technology to minimize EMI emissions from the device. The SSM3525 passes FCC Class B emissions testing with an unshielded 20 inch cable using ferrite bead-based filtering. For applications that have difficulty passing FCC Class B emission tests, the SSM3525 includes an ultralow EMI emissions mode that significantly reduces the radiated emissions at the Class D outputs, particularly above 100 MHz. Reducing the supply voltage greatly reduces radiated emissions.

OUTPUT MODULATION DESCRIPTION

The SSM3525 uses three-level, Σ-Δ output modulation. Each output can swing from ground to PV_{DD}, and vice versa. Ideally, when no input signal is present, the output differential voltage is 0 V because there is no need to generate a pulse. In a real-world situation, noise sources are always present.

Due to this constant presence of noise, a differential pulse is occasionally generated in response to this stimulus. A small amount of current flows into the inductive load when the differential pulse is generated. However, typically, the output differential voltage is 0 V. This feature ensures the current flowing through the inductive load is small.

When the user sends an input signal, an output pulse is generated to follow the input voltage. The differential pulse density is increased by raising the input signal level. Figure 78 depicts three-level, Σ-Δ output modulation with and without input stimulus.

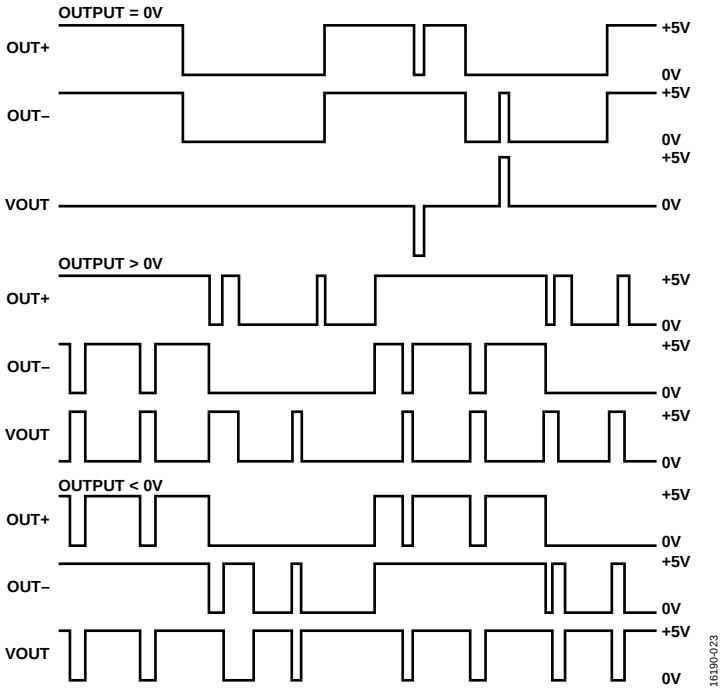

Figure 78. Three-Level, Σ-Δ Output Modulation With and Without Input Stimulus

BOOTSTRAP CAPACITORS

The output stage of the SSM3525 uses a high-side N-channel metal-oxide semiconductor (NMOS) driver, rather than a P-channel metal-oxide semiconductor (PMOS) driver. To generate the gate drive voltage for the high-side NMOS, a bootstrap capacitor for each output terminal acts as a floating power supply for the switching cycle. Use 0.22 µF capacitors to connect the appropriate output pin (OUT±) to the bootstrap pin (BST±). For example, connect a 0.22 µF capacitor between OUT+ and BST+ for bootstrapping the OUT+ pin. Similarly, connect another 0.22 µF capacitor between the OUT− and BST− pins for the OUT− pin.

POWER SUPPLY DECOUPLING

To ensure high efficiency, low THD, and high PSRR, proper power supply decoupling is necessary. Noise transients on the power supply lines are short duration voltage spikes. These spikes can contain frequency components that extend into the hundreds of megahertz. The power supply input must be decoupled with a low equivalent series inductance (ESL) and a low equivalent series resistance (ESR) bulk capacitor larger than 220 µF. For high frequency decoupling, place 1 µF capacitors as close as possible to the PVDD pins of the device.

OUTPUT EMI FILTERING

Additional EMI filtering may be required when the speaker traces and cables are long and present a significant capacitive load that can create additional draw from the amplifier. Typical power ferrites present a significant magnetic hysteresis cycle that affects THD performance and are not recommended for high performance designs. The NFZ series ferrite beads from Murata are recommended. These ferrite beads provide a closed hysteresis loop similar to an air coil with minimum impact on performance. The ferrite beads with output current rating ≥4 A rms, are recommended for this application. A 220 pF capacitor can be added between the output of the filter and ground to further attenuate high frequencies. Ensure the capacitor is properly sized so as not to affect idle power consumption or efficiency.

PCB COMPONENT PLACEMENT

Component selection and placement have great influence on system performance, both measured and subjective. Proper PVDD layout and decoupling is necessary to reach the specified level of performance, particularly at the highest power levels. The placement shown in Figure 79 ensures proper output stage decoupling for each channel, for minimum supply noise and maximum separation between channels. Additional bulk decoupling is necessary to reduce current ripple at low frequencies, and can be shared between several amplifiers in a multichannel solution.

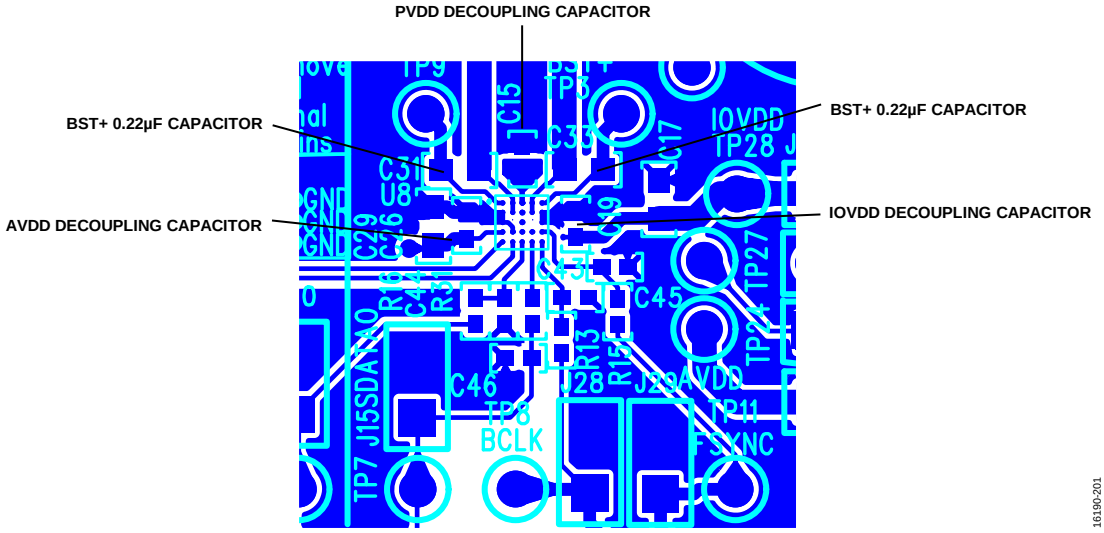

Figure 79. Recommended Component Placement {should PVDD, AVDD, and IOVDD be AV_{DD}, P_{VDD}, I_{OVDD}?

LAYOUT

As output power increases, take care to lay out PCB traces and wires properly among the amplifier, load, and power supply; a poor layout increases voltage drops, consequently decreasing efficiency. A good practice is to use short, wide PCB tracks to decrease voltage drops and minimize inductance. For the lowest dc resistance (DCR) and minimum inductance, ensure that trace widths for the speaker outputs are at least 200 mil for every inch of length and use 1 oz or 2 oz copper.

To maintain high output swing and high peak output power, the PCB traces that connect the output pins to the load and supply pins must be as wide as possible. In addition, good PCB layout isolates critical analog paths from sources of high interference. Separate high frequency circuits (analog and digital) from low frequency circuits.

PVDD and PGND carry most of the device current, and must be properly decoupled with multiple capacitors close to the device power supply and ground pins. To minimize ground bounce, use independent power planes to carry PVDD and PGND to the power supply. Proper grounding guidelines help improve audio performance, minimize crosstalk between channels, and prevent switching noise from coupling into the audio signal.

Properly designed multilayer PCBs can reduce electromagnetic emission and improve radio frequency (RF) immunity, compared with double-sided boards. A multilayer board allows a complete layer to be used for the ground plane, whereas the ground plane side of a double-sided board is often disrupted by signal traces.

If the system has separate analog and digital ground and power planes, the analog ground plane must be directly beneath the analog power plane, and, similarly, the digital ground plane must be directly beneath the digital power plane. There must be no overlap between the analog and digital ground planes or between the analog and digital power planes.

I²C CONTROL

The SSM3525 supports a 2-wire serial (I²C-compatible) microprocessor bus driving multiple peripherals. Two pins, serial data (SDA) and serial clock (SCL), carry information between the SSM3525 and the system I²C master controller. The SSM3525 is always a slave on the bus, meaning it cannot initiate a data transfer. Each slave device is recognized by a unique address. Using the ADDR pin provides the four device addresses, which are listed in Table 20. The address byte format is shown in Table 19. The address resides in the first seven bits of the I²C write. The LSB of this byte sets either a read or write operation. Logic Level 1 corresponds to a read operation, and Logic Level 0 corresponds to a write operation.

Connect 2.2 kΩ pull-up resistors on the lines connected to the SDA and SCL pins. The voltage on these signal lines must not be more than 5 V.

Addressing

Initially, each device on the I²C bus is in an idle state, monitoring the SDA and SCL lines for a start condition and the proper address. The I²C master initiates a data transfer by establishing a start condition, defined by a high to low transition on SDA while SCL remains high. This transition indicates that an address or data stream follows. All devices on the bus respond to the start condition and shift the next eight bits (the 7-bit address plus the R/$\overline{W}$ bit) MSB first. The device that recognizes the transmitted address responds by pulling the data line low during the ninth clock pulse. This ninth bit is an acknowledge bit. All other devices withdraw from the bus at this point and return to the idle condition. The device address for the SSM3525 is determined by the state of the ADDR pin. See Table 20 for four available addresses.

The R/$\overline{W}$ bit determines the direction of the data. A Logic 0 on the LSB of the first byte means the master writes information to the peripheral, whereas a Logic 1 means the master reads information from the peripheral after writing the subaddress and repeating the start address. A data transfer occurs until a stop condition is encountered. A stop condition occurs when SDA transitions from low to high while SCL is held high. The timing for the I²C port is shown in Figure 80.

Stop and start conditions can be detected at any stage during the data transfer. If these conditions are asserted out of sequence with normal read and write operations, the SSM3525 immediately jumps to the idle condition. During a given SCL high period, the user must issue only one start condition, one stop condition, or a single stop condition followed by a single start condition. If the user issues an invalid subaddress, the SSM3525 does not issue an acknowledge and returns to the idle condition. If the user exceeds the highest subaddress while in auto-increment mode, one of two actions is taken.

In read mode, the SSM3525 outputs the highest subaddress register contents until the master device issues a no acknowledge, indicating the end of a read. A no acknowledge condition is when the SDA line is not pulled low on the ninth clock pulse on SCL. If the highest subaddress location is reached while in write mode, the data for the invalid byte is not loaded into any subaddress register, a no acknowledge is issued by the SSM3525, and the device returns to the idle condition.

I²C Read and Write Operations

Figure 81 shows the timing of a single-word write operation. Every ninth clock, the SSM3525 issues an acknowledge (ACK) by pulling SDA low.

Figure 82 shows the timing of a burst mode write sequence. This figure shows an example in which the target destination registers are two bytes. The SSM3525 increments its subaddress register every byte because the requested subaddress corresponds to a register or memory area with a byte word length.

The timing of a single word read operation is shown in Figure 83. The first R/$\overline{W}$ bit is 0, indicating a write operation followed by the subaddress of the register to be read. After the SSM3525 acknowledges the receipt of the subaddress, the master must issue a repeated start command followed by the chip address byte with the R/$\overline{W}$ set to 1 (read). The SSM3525 acknowledges and puts 8-bit data on the SDA pin. The master then responds every ninth pulse with an acknowledge pulse to the SSM3525.

Figure 81 through Figure 84 use the following abbreviations:

- S is the start bit
- P is the stop bit
- A_M is the acknowledge by master
- A_S is the acknowledge by slave

Table 19. I²C Device Address Byte Format Using the ADDR Pin[1]

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	1	0	0	1	X	X	R/$\overline{W}$

[1] X means don't care.

Table 20. ADDR Pin to I²C Device Address Mapping

ADDR Pin	ADDR Voltage	I²C Address Bit 2	I²C Address Bit 1
GND	GND	0	0
Pull-Down 47 kΩ Resistor	0.25 × IOV_{DD}	0	1
Open	0.5 × IOV_{DD}	1	0
Pull-Up 47 kΩ Resistor	0.75 × IOV_{DD}	1	1
IOVDD	IOV_{DD}	Not applicable	Not applicable

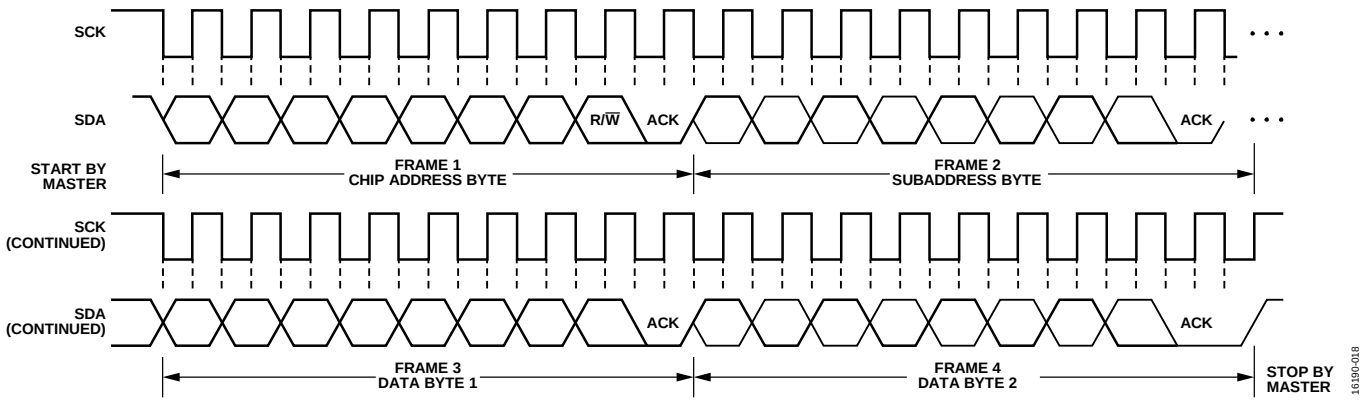

Figure 80. I²C Read/Write Timing

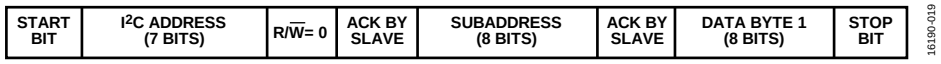

Figure 81. Single Word I²C Write Format

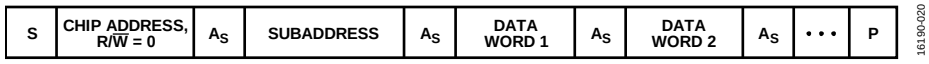

Figure 82. Burst Mode I²C Write Format

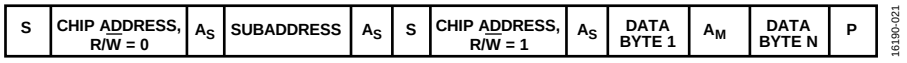

Figure 83. Single Word I²C Read Format

Figure 84. Burst Mode I²C Read Format

APPLICATIONS INFORMATION

Figure 64 shows typical application for a single channel using I²S/TDM input and I²C control. In a typical application, the PV_{DD} and IOV_{DD} are supplied externally. AV_{DD} can be generated using an internal regulator by setting the REG_EN bit in Register 0x04 to 1. Alternately, AV_{DD} can be provided externally and disabling the REG_EN bit. By default, the AV_{DD} regulator is disabled. The IOV_{DD} by default is set to 1.8 V and can be changed to 1.2 V by using the IOVDD_SEL bit in Register 0x20.

During power up, turn the PVDD supply on first, followed by IOV_{DD}. While powering off, turn off the IOVDD supply first, followed by PVDD. The IOV_{DD} must be stable before I²C commands are sent to the device. The digital input data can be 2-channel I²S or multichannel TDM format, and the desired format must be selected in the SAI control registers. Refer to the PCM Digital Audio Serial Interface section.

On power-up, the device stays in power-down; to enable the amplifier, the SPWDN bit in Register 0x20 must be set to 0. Once this bit is set to 0, the amplifier turns on and the output starts switching.

The slew rate for the output can be set to low EMI mode in Register 0x05. By default, the slew rate is set to normal mode. In low EMI mode, the output slew rate is reduced to lower the radiated emissions at the speaker output.

The device can be reset to default settings by writing 1 to the S_RST bit in Register 0x2E. This bit must be cleared by writing 0 to bring the device out of reset.

The PV_{DD} (V_{BAT}) sense cannot be powered down and is enabled by default. By default, the high pass filter is enabled and it is recommended to keep it enabled to block the dc from appearing at the speaker outputs.

The fault status register, 0x11, can be read to check for any fault conditions during operation.

FB1, FB2, C7, and C8 (see Figure 64) are recommended for filtering the switching noise and must be placed closer to the amplifier outputs to be effective.

SSM3525 I²C MODE REGISTER MAP (SSM3525_I2C_REGMAP) REGISTER SUMMARY

Table 21. SSM3525_I2C_REGMAP Register Summary

Reg	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	RW
0x00	VENDOR_ID	[7:0]	VENDOR								0x41	R
0x01	DEVICE_ID1	[7:0]	DEVICE1								0x35	R
0x02	DEVICE_ID2	[7:0]	DEVICE2								0x25	R
0x03	REVISION_ID	[7:0]	REVISION								0x01	R
0x04	REG_ENABLE	[7:0]	RESERVED							REG_EN	0x00	R/W
0x05	AMP_CTRL	[7:0]	SNS_HPF_BP	SNS_FS			RESERVED	EDGE	ANA_GAIN		0x22	R/W
0x06	DAC_CTRL	[7:0]	DAC_HV	DAC_MUTE	DAC_HPF	DAC_LPM	DAC_POL	DAC_FS			0x32	R/W
0x07	DAC_VOL	[7:0]	VOL								0x40	R/W
0x08	LIM_CTRL1	[7:0]	LIM_RRT		LIM_ATR		RESERVED	VBAT_TRACK	LIM_EN		0xA4	R/W
0x09	LIM_CTRL2	[7:0]	LIM_THRES					RESERVED	SLOPE		0x51	R/W
0x0A	LIM_CTRL3	[7:0]	VBAT_INF								0x22	R/W
0x0B	VBAT_LIM_CTRL1	[7:0]	VBAT_LIM_RRT		VBAT_LIM_ATR		RESERVED			VBAT_LIM_EN	0xA0	R/W
0x0C	VBAT_LIM_CTRL2	[7:0]	VBAT_THRES								0x22	R/W
0x0D	VBAT_LIM_CTRL3	[7:0]	VBAT_LIM_MAX_ATTN				VBAT_LIM_HOLD				0x65	R/W
0x0E	LIM_LINK	[7:0]	RESERVED				LIM_LINK4	LIM_LINK3	LIM_LINK2	LIM_LINK1	0x00	R/W
0x0F	DAC_CLIP	[7:0]	DAC_CLIP								0xFF	R/W
0x10	FAULT_CTRL	[7:0]	OTW_GAIN		MRCV	MAX_AR		ARCV_UV	ARCV_OT	ARCV_OC	0x18	R/W
0x11	STATUS	[7:0]	UVLO_VREG	UVLO_PVDD	LIM_EG	CLIP	AMP_OC	OTF	OTW	BAT_WARN	0x00	R
0x12	TEMP	[7:0]	TEMP								0x00	R
0x13	VBAT	[7:0]	VBAT								0x00	R
0x20	PWR_CTRL	[7:0]	RESERVED		VSNS_PWDN	ISNS_PWDN	RESERVED	TEMP_PWDN	IOVDD_SEL	SPWDN	0x05	R/W
0x21	PDM_CTRL	[7:0]	RESERVED			PDM_FS	RESERVED			PDM_MODE	0x00	R/W
0x22	SAI_CTRL1	[7:0]	SAI_DRV	TDM_BCLKS			BCLK_POL	FSYNC_MODE	SDATA_FMT	SAI_MODE	0x21	R/W
0x23	SAI_CTRL2	[7:0]	RESERVED			TDM_SLOT					0x00	R/W
0x24	SAI_PLACE1	[7:0]	RESERVED		P1_DAC		P1_SNS				0x01	R/W
0x25	SAI_PLACE2	[7:0]	RESERVED		P2_DAC		P2_SNS				0x21	R/W
0x26	SAI_PLACE3	[7:0]	RESERVED		P3_DAC		P3_SNS				0x21	R/W
0x27	SAI_PLACE4	[7:0]	RESERVED		P4_DAC		P4_SNS				0x21	R/W
0x28	SAI_PLACE5	[7:0]	RESERVED				P5_SNS				0x01	R/W
0x29	SAI_PLACE6	[7:0]	RESERVED				P6_SNS				0x01	R/W
0x2A	AGC_PLACE1	[7:0]	AGC_GAIN1_PLACE			AGC_GAIN1_SLOT					0x00	R/W
0x2B	AGC_PLACE2	[7:0]	AGC_GAIN2_PLACE			AGC_GAIN2_SLOT					0x00	R/W
0x2C	AGC_PLACE3	[7:0]	AGC_GAIN3_PLACE			AGC_GAIN3_SLOT					0x00	R/W
0x2D	AGC_PLACE4	[7:0]	AGC_GAIN4_PLACE			AGC_GAIN4_SLOT					0x00	R/W
0x2E	SOFT_RESET	[7:0]	RESERVED							S_RST	0x00	W

SSM3525 I²C MODE REGISTER MAP (SSM3525_I2C_REGMAP) REGISTER DETAILS

ADI VENDOR ID REGISTER

Address: 0x00, Reset: 0x41, Name: VENDOR_ID

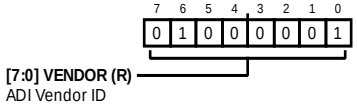

Table 22. Bit Descriptions for VENDOR_ID

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	VENDOR		ADI Vendor ID	0x41	R

DEVICE ID 1 REGISTER

Address: 0x01, Reset: 0x35, Name: DEVICE_ID1

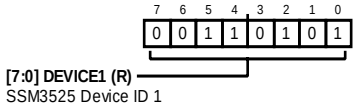

Table 23. Bit Descriptions for DEVICE_ID1

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	DEVICE1		SSM3525 Device ID 1	0x35	R

DEVICE ID 1 REGISTER

Address: 0x02, Reset: 0x25, Name: DEVICE_ID2

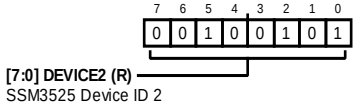

Table 24. Bit Descriptions for DEVICE_ID2

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	DEVICE2		SSM3525 Device ID 2	0x25	R

REVISION ID REGISTER

Address: 0x03, Reset: 0x01, Name: REVISION_ID

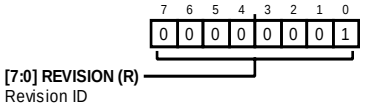

Table 25. Bit Descriptions for REVISION_ID

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	REVISION		Revision ID	0x1	R

REGULATOR ENABLE AND IOVDD SELECTION REGISTER

Address: 0x04, Reset: 0x00, Name: REG_ENABLE

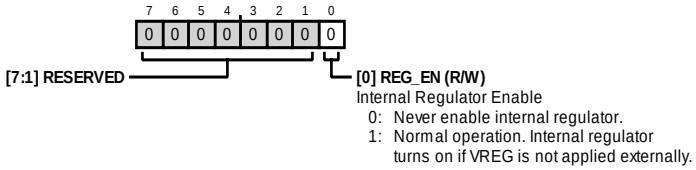

Table 26. Bit Descriptions for REG_ENABLE

Bits	Bit Name	Settings	Description	Reset	Access
[7:1]	RESERVED		Reserved.	0x0	R
0	REG_EN		Internal Regulator Enable	0x0	R/W
		0	Never enable internal regulator.		
		1	Normal operation. Internal regulator turns on if VREG is not applied externally.		

AMPLIFIER GAIN, EDGE CONTROL, AND SENSE SAMPLE RATE REGISTER

Address: 0x05, Reset: 0x22, Name: AMP_CTRL

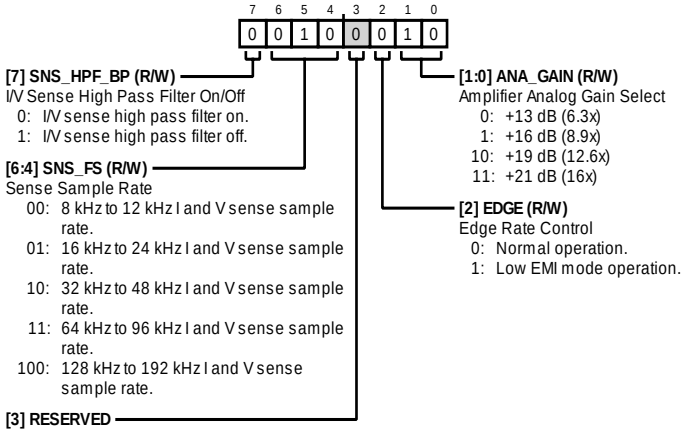

Table 27. Bit Descriptions for AMP_CTRL

Bits	Bit Name	Settings	Description	Reset	Access
7	SNS_HPF_BP		I/V Sense High Pass Filter On/Off	0x0	R/W
		0	I/V sense high pass filter on.		
		1	I/V sense high pass filter off.		
[6:4]	SNS_FS		Sense Sample Rate. The sense output sample rate can be set at a lower rate than the DAC sample rate. When the sense sample rate is less than the DAC sample rate, sense ADC samples repeat. The number of times the sample repeats is equal to the ratio of the DAC sample rate/sense sample rate.	0x2	R/W
		00	8 kHz to 12 kHz I and V sense sample rate.		
		01	16 kHz to 24 kHz I and V sense sample rate.		
		10	32 kHz to 48 kHz I and V sense sample rate.		
		11	64 kHz to 96 kHz I and V sense sample rate.		
		100	128 kHz to 192 kHz I and V sense sample rate.		
3	RESERVED		Reserved.	0x0	R
2	EDGE		Edge Rate Control. This controls the edge speed of the power stage. The low EMI operation mode reduces the edge speed, lowering EMI and power efficiency	0x0	R/W
		0	Normal operation.		
		1	Low EMI mode operation.		

Bits	Bit Name	Settings	Description	Reset	Access
[1:0]	ANA_GAIN		Amplifier Analog Gain Select	0x2	R/W
		0	+13 dB (6.3x)		
		1	+16 dB (8.9x)		
		10	+19 dB (12.6x)		
		11	+21 dB (16x)		

DAC CONTROL REGISTER

Address: 0x06, Reset: 0x32, Name: DAC_CTRL

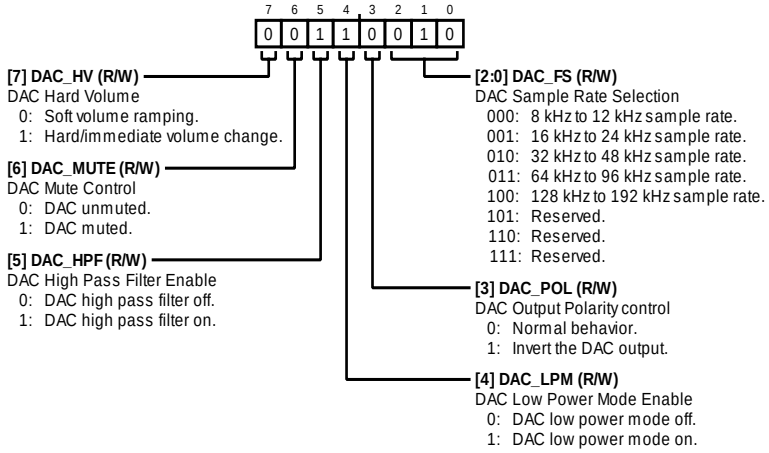

Table 28. Bit Descriptions for DAC_CTRL

Bits	Bit Name	Settings	Description	Reset	Access
7	DAC_HV		DAC Hard Volume	0x0	R/W
		0	Soft volume ramping.		
		1	Hard/immediate volume change.		
6	DAC_MUTE		DAC Mute Control	0x0	R/W
		0	DAC unmuted.		
		1	DAC muted.		
5	DAC_HPF		DAC High Pass Filter Enable	0x1	R/W
		0	DAC high pass filter off.		
		1	DAC high pass filter on.		
4	DAC_LPM		DAC Low Power Mode Enable	0x1	R/W
		0	DAC low power mode off.		
		1	DAC low power mode on.		
3	DAC_POL		DAC Output Polarity control	0x0	R/W
		0	Normal behavior.		
		1	Invert the DAC output.		
[2:0]	DAC_FS		DAC Sample Rate Selection	0x2	R/W
		000	8 kHz to 12 kHz sample rate.		
		001	16 kHz to 24 kHz sample rate.		
		010	32 kHz to 48 kHz sample rate.		
		011	64 kHz to 96 kHz sample rate.		
		100	128 kHz to 192 kHz sample rate.		
		101	Reserved.		
		110	Reserved.		
		111	Reserved.		

DAC VOLUME CONTROL REGISTER

Address: 0x07, Reset: 0x40, Name: DAC_VOL

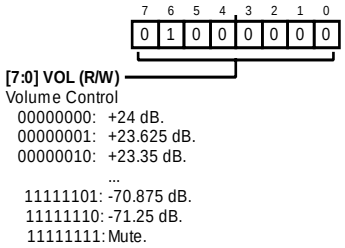

Table 29. Bit Descriptions for DAC_VOL

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	VOL		Volume Control	0x40	R/W
		00000000	+24 dB.		
		00000001	+23.625 dB.		
		00000010	+23.35 dB.		
		00000011	+22.875 dB.		
		00000100	+22.5 dB.		
		00000101	...		
		00111111	+0.375 dB.		
		01000000	0.		
		01000001	−0.375 dB.		
		01000010	...		
		11111101	−70.875 dB.		
		11111110	−71.25 dB.		
		11111111	Mute.		

AUDIO LIMITER CONTROL 1 REGISTER

Address: 0x08, Reset: 0xA4, Name: LIM_CTRL1

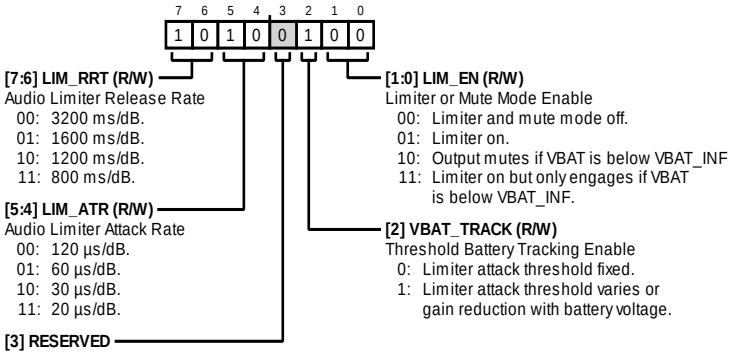

Table 30. Bit Descriptions for LIM_CTRL1

Bits	Bit Name	Settings	Description	Reset	Access
[7:6]	LIM_RRT		Audio Limiter Release Rate	0x2	R/W
		00	3200 ms/dB.		
		01	1600 ms/dB.		
		10	1200 ms/dB.		
		11	800 ms/dB.		
[5:4]	LIM_ATR		Audio Limiter Attack Rate	0x2	R/W
		00	120 µs/dB.		
		01	60 µs/dB.		
		10	30 µs/dB.		
		11	20 µs/dB.		
3	RESERVED		Reserved.	0x0	R
2	VBAT_TRACK		Threshold Battery Tracking Enable	0x1	R/W
		0	Limiter attack threshold fixed.		
		1	Limiter attack threshold varies or gain reduction with battery voltage.		
[1:0]	LIM_EN		Limiter or Mute Mode Enable	0x0	R/W
		00	Limiter and mute mode off.		
		01	Limiter on.		
		10	Output mutes if VBAT is below VBAT_INF.		
		11	Limiter on but only engages if VBAT is below VBAT_INF.		

AUDIO LIMITER CONTROL 2 REGISTER

Address: 0x09, Reset: 0x51, Name: LIM_CTRL2

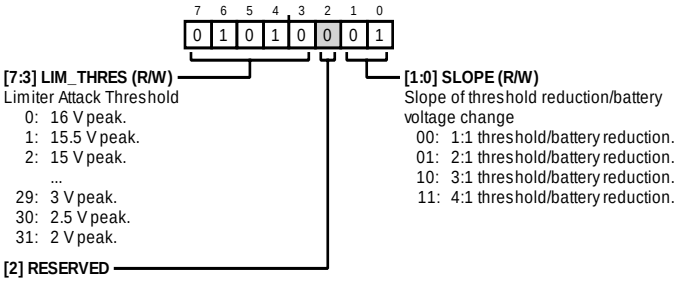

Table 31. Bit Descriptions for LIM_CTRL2

Bits	Bit Name	Settings	Description	Reset	Access
[7:3]	LIM_THRES		Limiter Attack Threshold	0xA	R/W
		0	16 V_{PEAK}.		
		1	15.5 V_{PEAK}.		
		2	15 V_{PEAK}.		
		3	14.5 V_{PEAK}.		
		4	14 V_{PEAK}.		
		5	13.5 V_{PEAK}.		
		6	13 V_{PEAK}.		
		7	12.5 V_{PEAK}.		
		8	12 V_{PEAK}.		
		9	11.5 V_{PEAK}.		
		10	11 V_{PEAK}.		
		11	10.5 V_{PEAK}.		
		12	10 V_{PEAK}.		
		13	9.5 V_{PEAK}.		
		14	9.25 V_{PEAK}.		
		15	9 V_{PEAK}.		
		16	8.75 V_{PEAK}.		
		17	8.5 V_{PEAK}.		
		18	8.25 V_{PEAK}.		
		19	8 V_{PEAK}.		
		20	7.5 V_{PEAK}.		
		21	7 V_{PEAK}.		
		22	6.5 V_{PEAK}.		
		23	6 V_{PEAK}.		
		24	5.5 V_{PEAK}.		
		25	5 V_{PEAK}.		
		26	4.5 V_{PEAK}.		
		27	4 V_{PEAK}.		
		28	3.5 V_{PEAK}.		
		29	3 V_{PEAK}.		
		30	2.5 V_{PEAK}.		
		31	2 V_{PEAK}.		
2	RESERVED		Reserved.	0x0	R
[1:0]	SLOPE		Slope of Threshold Reduction/Battery Voltage Change	0x1	R/W
		00	1:1 threshold/battery reduction.		
		01	2:1 threshold/battery reduction.		
		10	3:1 threshold/battery reduction.		
		11	4:1 threshold/battery reduction.		

AUDIO LIMITER CONTROL 3 REGISTER

Address: 0x0A, Reset: 0x22, Name: LIM_CTRL3

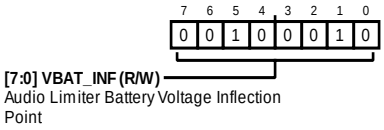

Table 32. Bit Descriptions for LIM_CTRL3

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	VBAT_INF		Audio Limiter Battery Voltage Inflection Point. The hexadecimal value corresponds to the battery or PVDD voltage at which the limiter either activates or starts reducing the limiter threshold. To convert the hexadecimal value to the corresponding battery voltage, see the PVDD (VBAT) Sensing section.	0x22	R/W

VBAT LIMITER CONTROL 1 REGISTER

Address: 0x0B, Reset: 0xA0, Name: VBAT_LIM_CTRL1

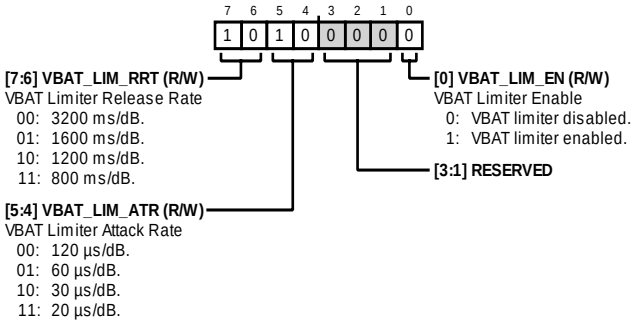

Table 33. Bit Descriptions for VBAT_LIM_CTRL1

Bits	Bit Name	Settings	Description	Reset	Access
[7:6]	VBAT_LIM_RRT		VBAT Limiter Release Rate	0x2	R/W
		00	3200 ms/dB.		
		01	1600 ms/dB.		
		10	1200 ms/dB.		
		11	800 ms/dB.		
[5:4]	VBAT_LIM_ATR		VBAT Limiter Attack Rate	0x2	R/W
		00	120 µs/dB.		
		01	60 µs/dB.		
		10	30 µs/dB.		
		11	20 µs/dB.		
[3:1]	RESERVED		Reserved.	0x0	R
0	VBAT_LIM_EN		VBAT Limiter Enable	0x0	R/W
		0	VBAT limiter disabled.		
		1	VBAT limiter enabled.		

VBAT LIMITER CONTROL 2 REGISTER

Address: 0x0C, Reset: 0x22, Name: VBAT_LIM_CTRL2

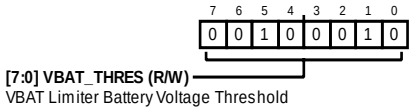

Table 34. Bit Descriptions for VBAT_LIM_CTRL2

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	VBAT_THRES		VBAT Limiter Battery Voltage Threshold. This is the threshold value in hexadecimal at which the VBAT limiter starts reducing the gain. To convert the hexadecimal value to the corresponding battery voltage refer to VBAT sensing section.	0x22	R/W

VBAT LIMITER CONTROL 3 REGISTER

Address: 0x0D, Reset: 0x65, Name: VBAT_LIM_CTRL3

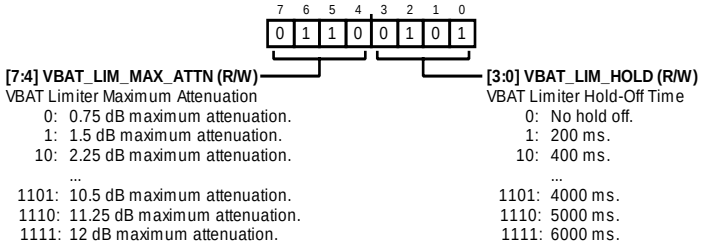

Table 35. Bit Descriptions for VBAT_LIM_CTRL3

Bits	Bit Name	Settings	Description	Reset	Access
[7:4]	VBAT_LIM_MAX_ATTN		VBAT Limiter Maximum Attenuation	0x6	R/W
		0	0.75 dB maximum attenuation.		
		1	1.5 dB maximum attenuation.		
		10	2.25 dB maximum attenuation.		
		11	3 dB maximum attenuation.		
		100	3.75 dB maximum attenuation.		
		101	4.5 dB maximum attenuation.		
		110	5.25 dB maximum attenuation.		
		111	6 dB maximum attenuation.		
		1000	6.75 dB maximum attenuation.		
		1001	7.5 dB maximum attenuation.		
		1010	8.25 dB maximum attenuation.		
		1011	9 dB maximum attenuation.		
		1100	9.75 dB maximum attenuation.		
		1101	10.5 dB maximum attenuation.		
		1110	11.25 dB maximum attenuation.		
		1111	12 dB maximum attenuation.		
[3:0]	VBAT_LIM_HOLD		VBAT Limiter Hold-Off Time'	0x5	R/W
		0	No hold off.		
		1	200 ms.		
		10	400 ms.		
		11	600 ms.		
		100	800 ms.		
		101	1000 ms.		
		110	1200 ms.		
		111	1400 ms.		
		1000	1600 ms.		
		1001	1800 ms.		

Bits	Bit Name	Settings	Description	Reset	Access
		1010	2000 ms.		
		1011	2500 ms.		
		1100	3000 ms.		
		1101	4000 ms.		
		1110	5000 ms.		
		1111	6000 ms.		

LIMITER LINK CONTROL REGISTER

Address: 0x0E, Reset: 0x00, Name: LIM_LINK

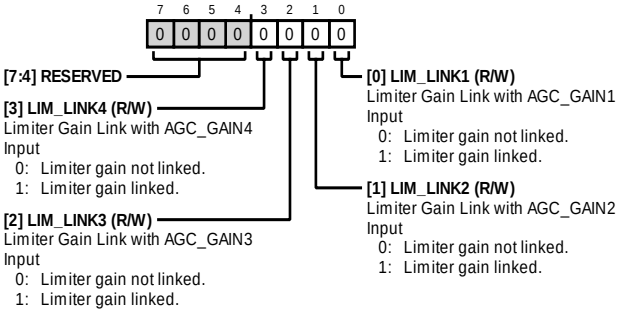

Table 36. Bit Descriptions for LIM_LINK

Bits	Bit Name	Settings	Description	Reset	Access
[7:4]	RESERVED		Reserved.	0x0	R
3	LIM_LINK4		Limiter Gain Link with AGC_GAIN4 Input	0x0	R/W
		0	Limiter gain not linked.		
		1	Limiter gain linked.		
2	LIM_LINK3		Limiter Gain Link with AGC_GAIN3 Input	0x0	R/W
		0	Limiter gain not linked.		
		1	Limiter gain linked.		
1	LIM_LINK2		Limiter Gain Link with AGC_GAIN2 Input	0x0	R/W
		0	Limiter gain not linked.		
		1	Limiter gain linked.		
0	LIM_LINK1		Limiter Gain Link with AGC_GAIN1 Input	0x0	R/W
		0	Limiter gain not linked.		
		1	Limiter gain linked.		

DAC CLIP POINT CONTROL REGISTER

Address: 0x0F, Reset: 0xFF, Name: DAC_CLIP

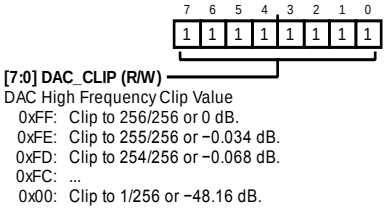

Table 37. Bit Descriptions for DAC_CLIP

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	DAC_CLIP		DAC High Frequency Clip Value	0xFF	R/W
		0xFF	Clip to 256/256 or 0 dB.		
		0xFE	Clip to 255/256 or −0.034 dB.		
		0xFD	Clip to 254/256 or −0.068 dB.		
		0xFC	...		
		0x00	Clip to 1/256 or −48.16 dB.		

FAULT CONTROL REGISTER

Address: 0x10, Reset: 0x18, Name: FAULT_CTRL

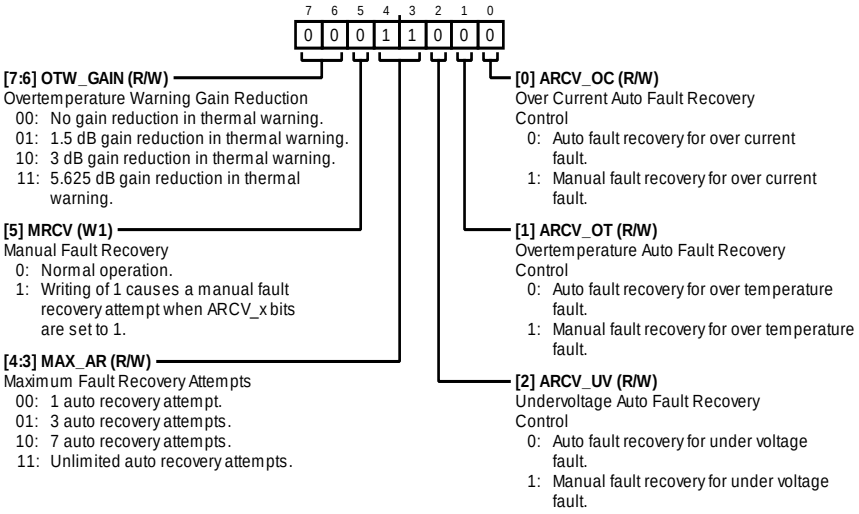

Table 38. Bit Descriptions for FAULT_CTRL

Bits	Bit Name	Settings	Description	Reset	Access
[7:6]	OTW_GAIN		Overtemperature Warning Gain Reduction	0x0	R/W
		00	No gain reduction in thermal warning.		
		01	1.5 dB gain reduction in thermal warning.		
		10	3 dB gain reduction in thermal warning.		
		11	5.625 dB gain reduction in thermal warning.		
5	MRCV		Manual Fault Recovery	0x0	W1
		0	Normal operation.		
		1	Writing 1 causes a manual fault recovery attempt when ARCV_x bits are set to 1.		
[4:3]	MAX_AR		Maximum Fault recovery Attempts. The maximum auto recovery register determines how many attempts at auto recovery are performed.	0x3	R/W
		00	1 auto recovery attempt.		
		01	3 auto recovery attempts.		
		10	7 auto recovery attempts.		
		11	Unlimited auto recovery attempts.		
2	ARCV_UV		Undervoltage Auto Fault Recovery Control	0x0	R/W
		0	Auto fault recovery for undervoltage fault.		
		1	Manual fault recovery for undervoltage fault.		
1	ARCV_OT		Overtemperature Auto Fault Recovery Control	0x0	R/W
		0	Auto fault recovery for overtemperature fault.		
		1	Manual fault recovery for overtemperature fault.		
0	ARCV_OC		Over Current Auto Fault Recovery Control	0x0	R/W
		0	Auto fault recovery for over current fault.		
		1	Manual fault recovery for over current fault.		

CHIP STATUS REGISTER

Address: 0x11, Reset: 0x00, Name: STATUS

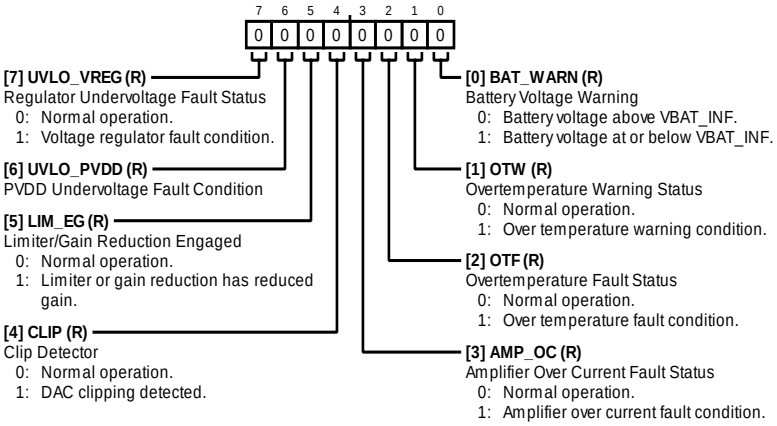

Table 39. Bit Descriptions for STATUS

Bits	Bit Name	Settings	Description	Reset	Access
7	UVLO_VREG		Regulator Undervoltage Fault Status	0x0	R
		0	Normal operation.		
		1	Voltage regulator fault condition.		
6	UVLO_PVDD		PVDD Undervoltage Fault Condition	0x0	R
5	LIM_EG		Limiter/Gain Reduction Engaged	0x0	R
		0	Normal operation.		
		1	Limiter or gain reduction has reduced gain.		
4	CLIP		Clip Detector	0x0	R
		0	Normal operation.		
		1	DAC clipping detected.		
3	AMP_OC		Amplifier Over Current Fault Status	0x0	R
		0	Normal operation.		
		1	Amplifier over current fault condition.		
2	OTF		Overtemperature Fault Status	0x0	R
		0	Normal operation.		
		1	Overtemperature fault condition.		
1	OTW		Overtemperature Warning Status	0x0	R
		0	Normal operation.		
		1	Overtemperature warning condition.		
0	BAT_WARN		Battery Voltage Warning	0x0	R
		0	Battery voltage above VBAT_INF.		
		1	Battery voltage at or below VBAT_INF.		

TEMPERATURE SENSOR VALUE REGISTER

Address: 0x12, Reset: 0x00, Name: TEMP

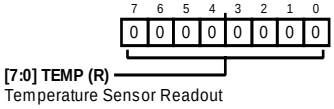

Table 40. Bit Descriptions for TEMP

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	TEMP		Temperature Sensor Readout. To calculate actual temperature in degrees Celsius, convert the TEMP hexadecimal value to decimal and then subtract 60.	0x0	R

PVDD/VBAT ADC VALUE REGISTER

Address: 0x13, Reset: 0x00, Name: VBAT

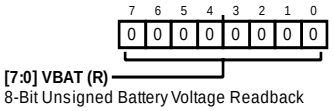

Table 41. Bit Descriptions for VBAT

Bits	Bit Name	Settings	Description	Reset	Access
[7:0]	VBAT		8-Bit Unsigned Battery Voltage Readback. To calculate this value in volts. Convert the hexadecimal value to decimal, and then voltage = 4 + 14 × decimal value/255.	0x0	R

MASTER AND BLOCK POWER CONTROL REGISTER

Address: 0x20, Reset: 0x05, Name: PWR_CTRL

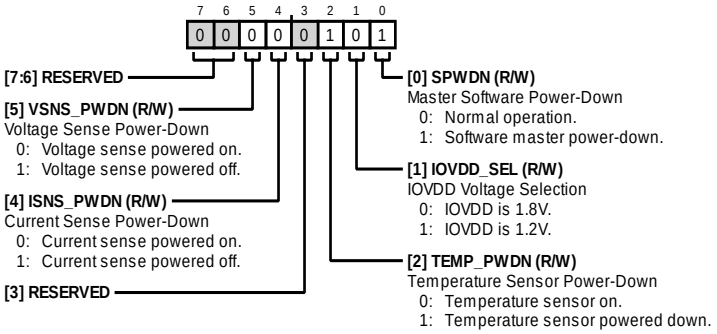

Table 42. Bit Descriptions for PWR_CTRL

Bits	Bit Name	Settings	Description	Reset	Access
[7:6]	RESERVED		Reserved.	0x0	R
5	VSNS_PWDN		Voltage Sense Power-Down	0x0	R/W
		0	Voltage sense powered on.		
		1	Voltage sense powered off.		
4	ISNS_PWDN		Current Sense Power-Down	0x0	R/W
		0	Current sense powered on.		
		1	Current sense powered off.		
3	RESERVED		Reserved.	0x0	R
2	TEMP_PWDN		Temperature Sensor Power-Down	0x1	R/W
		0	Temperature sensor on.		
		1	Temperature sensor powered down.		
1	IOVDD_SEL		IOV_{DD} Voltage Selection	0x0	R/W
		0	IOV_{DD} is 1.8 V.		
		1	IOV_{DD} is 1.2 V.		
0	SPWDN		Master Software Power-Down. Software power-down puts all blocks except the I^2C interface in a low power state.	0x1	R/W
		0	Normal operation.		
		1	Software master power-down.		

PDM CONTROL REGISTER

Address: 0x21, Reset: 0x00, Name: PDM_CTRL

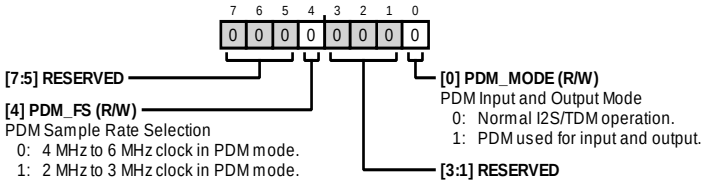

Table 43. Bit Descriptions for PDM_CTRL

Bits	Bit Name	Settings	Description	Reset	Access
[7:5]	RESERVED		Reserved.	0x0	R
4	PDM_FS		PDM Sample Rate Selection	0x0	R/W
		0	4 MHz to 6 MHz clock in PDM mode.		
		1	2 MHz to 3 MHz clock in PDM mode.		
[3:1]	RESERVED		Reserved.	0x0	R
0	PDM_MODE		PDM Input and Output Mode	0x0	R/W
		0	Normal I²S/TDM operation.		
		1	PDM used for input and output.		

SERIAL INTERFACE CONTROL 1 REGISTER

Address: 0x22, Reset: 0x21, Name: SAI_CTRL1

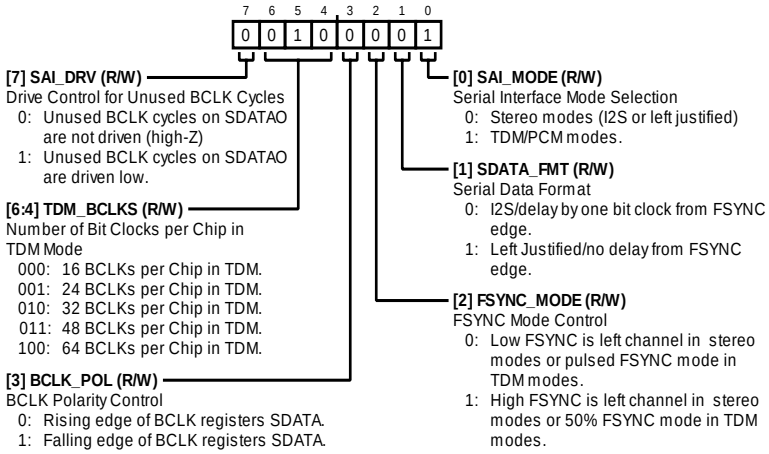

Table 44. Bit Descriptions for SAI_CTRL1

Bits	Bit Name	Settings	Description	Reset	Access
7	SAI_DRV		Drive Control for Unused BCLK Cycles	0x0	R/W
		0	Unused BCLK cycles on SDATAO are not driven (high-Z).		
		1	Unused BCLK cycles on SDATAO are driven low.		
[6:4]	TDM_BCLKS		Number of Bit Clocks per Chip in TDM Mode. Any number of bit clock cycles per FSYNC can be used in stereo modes (I²S or left justified) or in TDM mode with only one chip. When in TDM mode and having multiple chips on the TDM bus, the number of bit clocks per chip must be defined.	0x2	R/W
		000	16 BCLKs per chip in TDM.		
		001	24 BCLKs per chip in TDM.		
		010	32 BCLKs per chip in TDM.		
		011	48 BCLKs per chip in TDM.		
		100	64 BCLKs per chip in TDM.		
3	BCLK_POL		BCLK Polarity Control	0x0	R/W
		0	Rising edge of BCLK registers SDATA.		
		1	Falling edge of BCLK registers SDATA.		

Bits	Bit Name	Settings	Description	Reset	Access
2	FSYNC_MODE		FSYNC Mode Control	0x0	R/W
		0	Low FSYNC is left channel in stereo modes or pulsed FSYNC mode in TDM modes.		
		1	High FSYNC is left channel in stereo modes or 50% FSYNC mode in TDM modes.		
1	SDATA_FMT		Serial Data Format	0x0	R/W
		0	I^2S/delay by one bit clock from FSYNC edge.		
		1	Left Justified/no delay from FSYNC edge.		
0	SAI_MODE		Serial Interface Mode Selection	0x1	R/W
		0	Stereo modes (I^2S or left justified)		
		1	TDM/PCM modes.		

SERIAL INTERFACE CONTROL 2 REGISTER

Address: 0x23, Reset: 0x00, Name: SAI_CTRL2

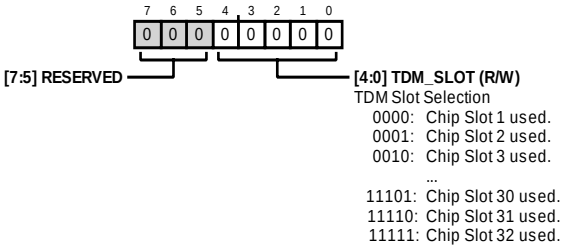

Table 45. Bit Descriptions for SAI_CTRL2

Bits	Bit Name	Settings	Description	Reset	Access
[7:5]	RESERVED		Reserved.	0x0	R
[4:0]	TDM_SLOT		TDM Slot Selection	0x0	R/W
		0000	Chip Slot 1 used.		
		0001	Chip Slot 2 used.		
		0010	Chip Slot 3 used.		
		0011	Chip Slot 4 used.		
		0100	Chip Slot 5 used.		
		0101	Chip Slot 6 used.		
		0110	Chip Slot 7 used.		
		0111	Chip Slot 8 used.		
		1000	Chip Slot 9 used.		
		1001	Chip Slot 10 used.		
		1010	Chip Slot 11 used.		
		1011	Chip Slot 12 used.		
		1100	Chip Slot 13 used.		
		1101	Chip Slot 14 used.		
		1110	Chip Slot 15 used.		
		1111	Chip Slot 16 used.		
		10000	Chip Slot 17 used.		
		10001	Chip Slot 18 used.		
		10010	Chip Slot 19 used.		
		10011	Chip Slot 20 used.		
		10100	Chip Slot 21 used.		
		10101	Chip Slot 22 used.		
		10110	Chip Slot 23 used.		
		10111	Chip Slot 24 used.		
		11000	Chip Slot 25 used.		
		11001	Chip Slot 26 used.		
		11010	Chip Slot 27 used.		

Bits	Bit Name	Settings	Description	Reset	Access
		11011	Chip Slot 28 used.		
		11100	Chip Slot 29 used.		
		11101	Chip Slot 30 used.		
		11110	Chip Slot 31 used.		
		11111	Chip Slot 32 used.		

SERIAL INTERFACE PLACEMENT CONTROL 1 REGISTER

Address: 0x24, Reset: 0x01, Name: SAI_PLACE1

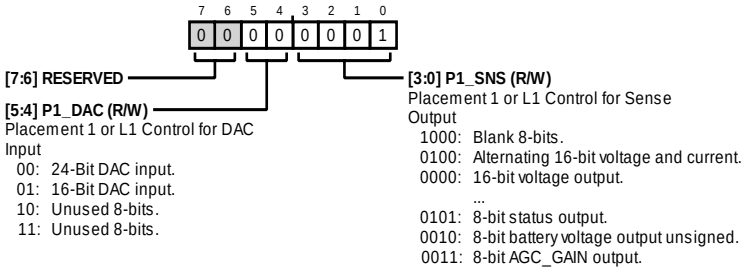

Table 46. Bit Descriptions for SAI_PLACE1

Bits	Bit Name	Settings	Description	Reset	Access
[7:6]	RESERVED		Reserved.	0x0	R
[5:4]	P1_DAC		Placement 1 or L1 Control for DAC Input	0x0	R/W
		00	24-bit DAC input.		
		01	16-bit DAC input.		
		10	Unused 8-bits.		
		11	Unused 8-bits.		
[3:0]	P1_SNS		Placement 1 or L1 Control for Sense Output	0x1	R/W
		1000	Blank 8-bits.		
		0100	Alternating 16-bit voltage and current.		
		0000	16-bit voltage output.		
		0001	16-bit current output.		
		0110	8-bit V/I marker and status.		
		0111	8-bit temperature output.		
		0101	8-bit status output.		
		0010	8-bit battery voltage output unsigned.		
		0011	8-bit AGC_GAIN output.		

SERIAL INTERFACE PLACEMENT CONTROL 2 REGISTER

Address: 0x25, Reset: 0x21, Name: SAI_PLACE2

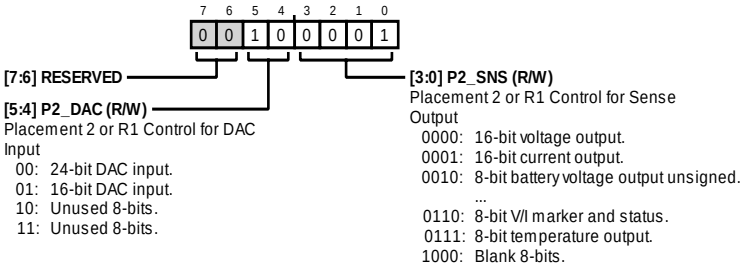

Table 47. Bit Descriptions for SAI_PLACE2

Bits	Bit Name	Settings	Description	Reset	Access
[7:6]	RESERVED		Reserved.	0x0	R
[5:4]	P2_DAC		Placement 2 or R1 Control for DAC Input	0x2	R/W
		00	24-bit DAC input.		
		01	16-bit DAC input.		
		10	Unused 8-bits.		
		11	Unused 8-bits.		
[3:0]	P2_SNS		Placement 2 or R1 Control for Sense Output	0x1	R/W
		0000	16-bit voltage output.		
		0001	16-bit current output.		
		0010	8-bit battery voltage output unsigned.		
		0011	8-bit AGC_GAIN output.		
		0100	Alternating 16-bit voltage and current.		
		0101	8-bit status output.		
		0110	8-bit V/I marker and status.		
		0111	8-bit temperature output.		
		1000	Blank 8-bits.		

SERIAL INTERFACE PLACEMENT CONTROL 3 REGISTER

Address: 0x26, Reset: 0x21, Name: SAI_PLACE3

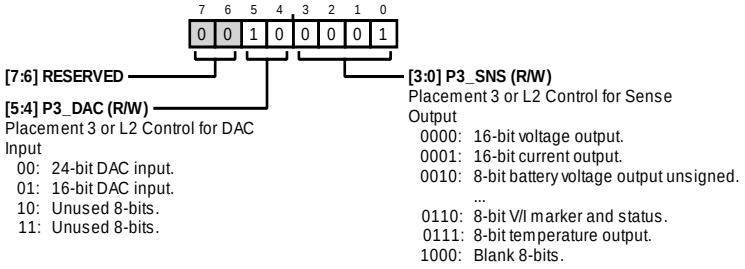

Table 48. Bit Descriptions for SAI_PLACE3

Bits	Bit Name	Settings	Description	Reset	Access
[7:6]	RESERVED		Reserved.	0x0	R
[5:4]	P3_DAC		Placement 3 or L2 Control for DAC Input	0x2	R/W
		00	24-bit DAC input.		
		01	16-bit DAC input.		
		10	Unused 8-bits.		
		11	Unused 8-bits.		

Bits	Bit Name	Settings	Description	Reset	Access
[3:0]	P3_SNS		Placement 3 or L2 Control for Sense Output	0x1	R/W
		0000	16-bit voltage output.		
		0001	16-bit current output.		
		0010	8-bit battery voltage output unsigned.		
		0011	8-bit AGC_GAIN output.		
		0100	Alternating 16-bit voltage and current.		
		0101	8-bit status output.		
		0110	8-bit V/I marker and status.		
		0111	8-bit temperature output.		
		1000	Blank 8-bits.		

SERIAL INTERFACE PLACEMENT CONTROL 4 REGISTER

Address: 0x27, Reset: 0x21, Name: SAI_PLACE4

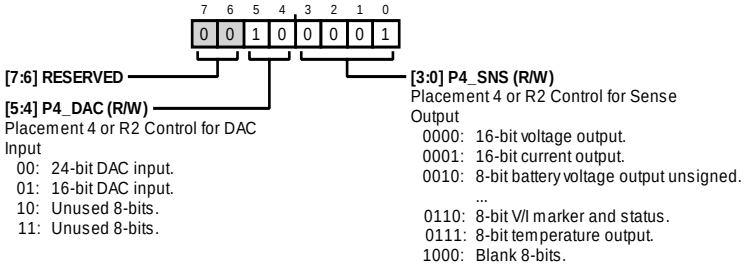

Table 49. Bit Descriptions for SAI_PLACE4

Bits	Bit Name	Settings	Description	Reset	Access
[7:6]	RESERVED		Reserved.	0x0	R
[5:4]	P4_DAC		Placement 4 or R2 Control for DAC Input	0x2	R/W
		00	24-bit DAC input.		
		01	16-bit DAC input.		
		10	Unused 8-bits.		
		11	Unused 8-bits.		
[3:0]	P4_SNS		Placement 4 or R2 Control for Sense Output	0x1	R/W
		0000	16-bit voltage output.		
		0001	16-bit current output.		
		0010	8-bit battery voltage output unsigned.		
		0011	8-bit AGC_GAIN output.		
		0100	Alternating 16-bit voltage and current.		
		0101	8-bit status output.		
		0110	8-bit V/I marker and status.		
		0111	8-bit temperature output.		
		1000	Blank 8-bits.		

SERIAL INTERFACE PLACEMENT CONTROL 5 REGISTER

Address: 0x28, Reset: 0x01, Name: SAI_PLACE5

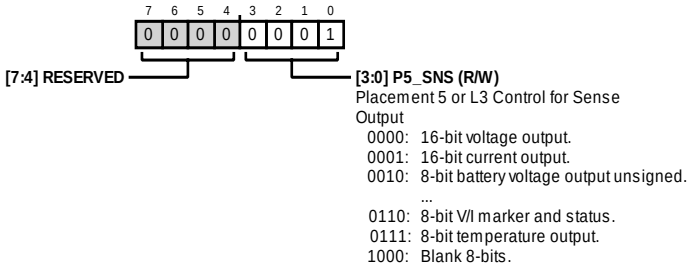

Table 50. Bit Descriptions for SAI_PLACE5

Bits	Bit Name	Settings	Description	Reset	Access
[7:4]	RESERVED		Reserved.	0x0	R
[3:0]	P5_SNS		Placement 5 or L3 Control for Sense Output	0x1	R/W
		0000	16-bit voltage output.		
		0001	16-bit current output.		
		0010	8-bit battery voltage output unsigned.		
		0011	8-bit AGC_GAIN output.		
		0100	Alternating 16-bit voltage and current.		
		0101	8-bit status output.		
		0110	8-bit V/I marker and status.		
		0111	8-bit temperature output.		
		1000	Blank 8-bits.		

SERIAL INTERFACE PLACEMENT CONTROL 6 REGISTER

Address: 0x29, Reset: 0x01, Name: SAI_PLACE6

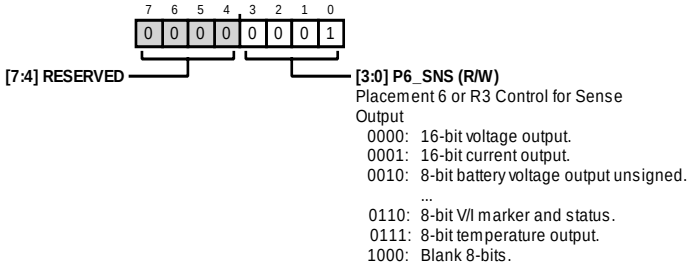

Table 51. Bit Descriptions for SAI_PLACE6

Bits	Bit Name	Settings	Description	Reset	Access
[7:4]	RESERVED		Reserved.	0x0	R
[3:0]	P6_SNS		Placement 6 or R3 Control for Sense Output	0x1	R/W
		0000	16-bit voltage output.		
		0001	16-bit current output.		
		0010	8-bit battery voltage output unsigned.		
		0011	8-bit AGC_GAIN output.		
		0100	Alternating 16-bit voltage and current.		
		0101	8-bit status output.		
		0110	8-bit V/I marker and status.		
		0111	8-bit temperature output.		
		1000	Blank 8-bits.		

AGC_GAIN1 INPUT DATA PLACEMENT REGISTER

Address: 0x2A, Reset: 0x00, Name: AGC_PLACE1

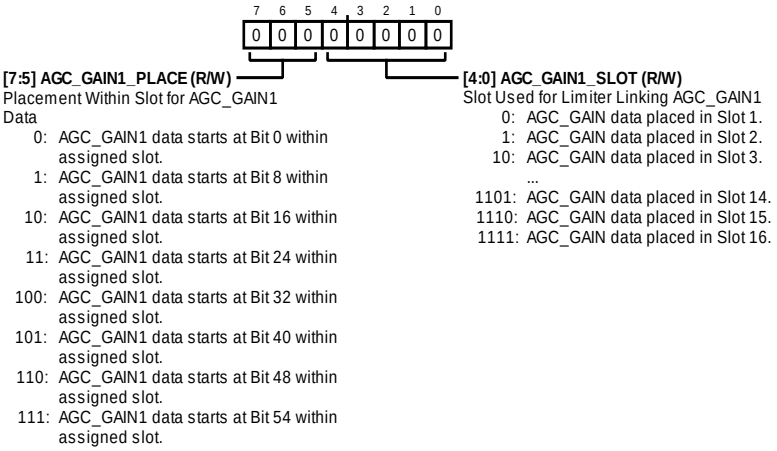

Table 52. Bit Descriptions for AGC_PLACE1

Bits	Bit Name	Settings	Description	Reset	Access
[7:5]	AGC_GAIN1_PLACE		Placement Within Slot for AGC_GAIN1 Data	0x0	R/W
		0	AGC_GAIN1 data starts at Bit 0 within assigned slot.		
		1	AGC_GAIN1 data starts at Bit 8 within assigned slot.		
		10	AGC_GAIN1 data starts at Bit 16 within assigned slot.		
		11	AGC_GAIN1 data starts at Bit 24 within assigned slot.		
		100	AGC_GAIN1 data starts at Bit 32 within assigned slot.		
		101	AGC_GAIN1 data starts at Bit 40 within assigned slot.		
		110	AGC_GAIN1 data starts at Bit 48 within assigned slot.		
		111	AGC_GAIN1 data starts at Bit 54 within assigned slot.		
[4:0]	AGC_GAIN1_SLOT		Slot Used for Limiter Linking AGC_GAIN1	0x0	R/W
		0	AGC_GAIN data placed in Slot 1.		
		1	AGC_GAIN data placed in Slot 2.		
		10	AGC_GAIN data placed in Slot 3.		
		11	AGC_GAIN data placed in Slot 4.		
		100	AGC_GAIN data placed in Slot 5.		
		101	AGC_GAIN data placed in Slot 6.		
		110	AGC_GAIN data placed in Slot 7.		
		111	AGC_GAIN data placed in Slot 8.		
		1000	AGC_GAIN data placed in Slot 9.		
		1001	AGC_GAIN data placed in Slot 10.		
		1010	AGC_GAIN data placed in Slot 11.		
		1011	AGC_GAIN data placed in Slot 12.		
		1100	AGC_GAIN data placed in Slot 13.		
		1101	AGC_GAIN data placed in Slot 14.		
		1110	AGC_GAIN data placed in Slot 15.		
		1111	AGC_GAIN data placed in Slot 16.		

AGC_GAIN2 INPUT DATA PLACEMENT REGISTER

Address: 0x2B, Reset: 0x00, Name: AGC_PLACE2

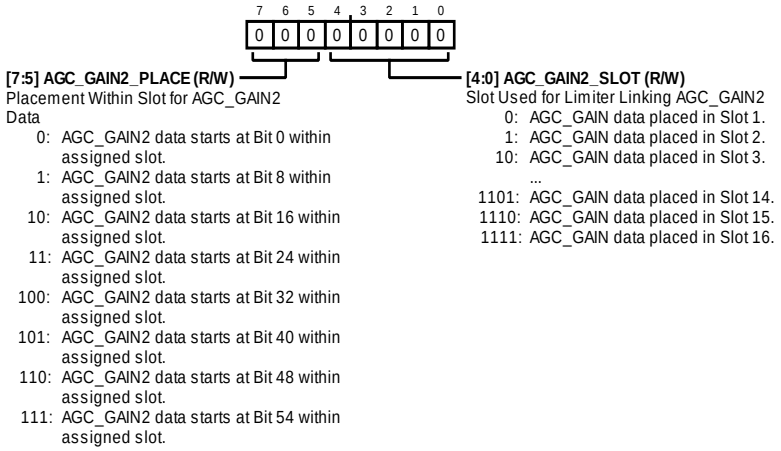

Table 53. Bit Descriptions for AGC_PLACE2

Bits	Bit Name	Settings	Description	Reset	Access
[7:5]	AGC_GAIN2_PLACE		Placement Within Slot for AGC_GAIN2 Data	0x0	R/W
		0	AGC_GAIN2 data starts at Bit 0 within assigned slot.		
		1	AGC_GAIN2 data starts at Bit 8 within assigned slot.		
		10	AGC_GAIN2 data starts at Bit 16 within assigned slot.		
		11	AGC_GAIN2 data starts at Bit 24 within assigned slot.		
		100	AGC_GAIN2 data starts at Bit 32 within assigned slot.		
		101	AGC_GAIN2 data starts at Bit 40 within assigned slot.		
		110	AGC_GAIN2 data starts at Bit 48 within assigned slot.		
		111	AGC_GAIN2 data starts at Bit 54 within assigned slot.		
[4:0]	AGC_GAIN2_SLOT		Slot Used for Limiter Linking AGC_GAIN2	0x0	R/W
		0	AGC_GAIN data placed in Slot 1.		
		1	AGC_GAIN data placed in Slot 2.		
		10	AGC_GAIN data placed in Slot 3.		
		11	AGC_GAIN data placed in Slot 4.		
		100	AGC_GAIN data placed in Slot 5.		
		101	AGC_GAIN data placed in Slot 6.		
		110	AGC_GAIN data placed in Slot 7.		
		111	AGC_GAIN data placed in Slot 8.		
		1000	AGC_GAIN data placed in Slot 9.		
		1001	AGC_GAIN data placed in Slot 10.		
		1010	AGC_GAIN data placed in Slot 11.		
		1011	AGC_GAIN data placed in Slot 12.		
		1100	AGC_GAIN data placed in Slot 13.		
		1101	AGC_GAIN data placed in Slot 14.		
		1110	AGC_GAIN data placed in Slot 15.		
		1111	AGC_GAIN data placed in Slot 16.		

AGC_GAIN3 INPUT DATA PLACEMENT REGISTER

Address: 0x2C, Reset: 0x00, Name: AGC_PLACE3

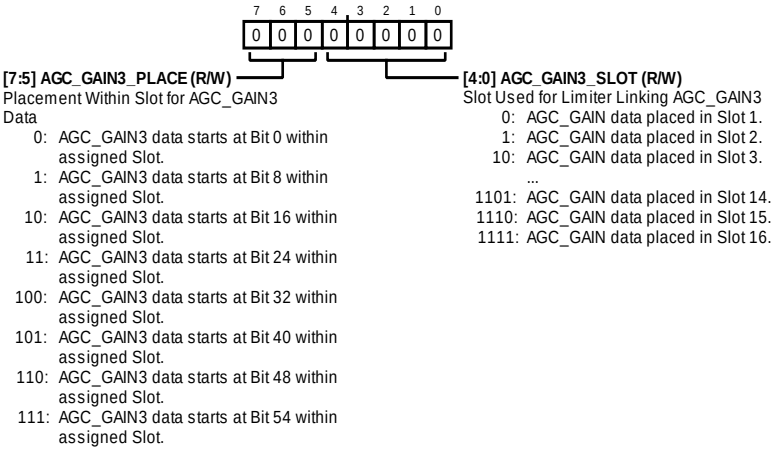

Table 54. Bit Descriptions for AGC_PLACE3

Bits	Bit Name	Settings	Description	Reset	Access
[7:5]	AGC_GAIN3_PLACE		Placement within slot for AGC_GAIN3 data	0x0	R/W
		0	AGC_GAIN3 data starts at Bit 0 within assigned slot.		
		1	AGC_GAIN3 data starts at Bit 8 within assigned slot.		
		10	AGC_GAIN3 data starts at Bit 16 within assigned slot.		
		11	AGC_GAIN3 data starts at Bit 24 within assigned slot.		
		100	AGC_GAIN3 data starts at Bit 32 within assigned slot.		
		101	AGC_GAIN3 data starts at Bit 40 within assigned slot.		
		110	AGC_GAIN3 data starts at Bit 48 within assigned slot.		
		111	AGC_GAIN3 data starts at Bit 54 within assigned slot.		
[4:0]	AGC_GAIN3_SLOT		Slot Used for Limiter Linking AGC_GAIN3	0x0	R/W
		0	AGC_GAIN data placed in Slot 1.		
		1	AGC_GAIN data placed in Slot 2.		
		10	AGC_GAIN data placed in Slot 3.		
		11	AGC_GAIN data placed in Slot 4.		
		100	AGC_GAIN data placed in Slot 5.		
		101	AGC_GAIN data placed in Slot 6.		
		110	AGC_GAIN data placed in Slot 7.		
		111	AGC_GAIN data placed in Slot 8.		
		1000	AGC_GAIN data placed in Slot 9.		
		1001	AGC_GAIN data placed in Slot 10.		
		1010	AGC_GAIN data placed in Slot 11.		
		1011	AGC_GAIN data placed in Slot 12.		
		1100	AGC_GAIN data placed in Slot 13.		
		1101	AGC_GAIN data placed in Slot 14.		
		1110	AGC_GAIN data placed in Slot 15.		
		1111	AGC_GAIN data placed in Slot 16.		

AGC_GAIN4 INPUT DATA PLACEMENT REGISTER

Address: 0x2D, Reset: 0x00, Name: AGC_PLACE4

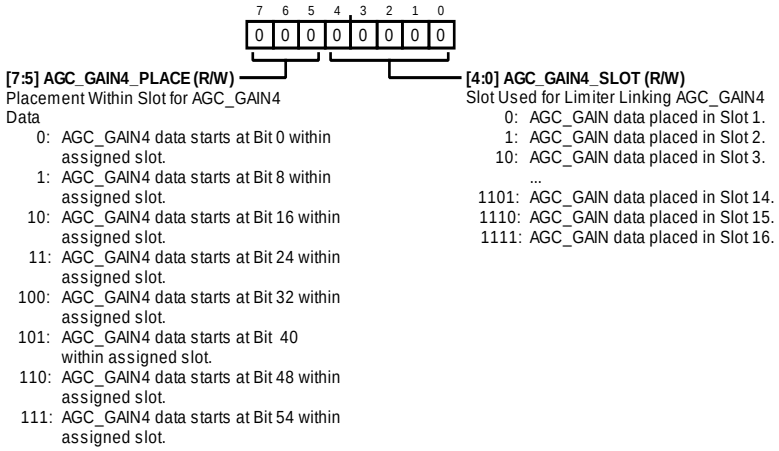

Table 55. Bit Descriptions for AGC_PLACE4

Bits	Bit Name	Settings	Description	Reset	Access
[7:5]	AGC_GAIN4_PLACE		Placement Within Slot for AGC_GAIN4 Data	0x0	R/W
		0	AGC_GAIN4 data starts at Bit 0 within assigned slot.		
		1	AGC_GAIN4 data starts at Bit 8 within assigned slot.		
		10	AGC_GAIN4 data starts at Bit 16 within assigned slot.		
		11	AGC_GAIN4 data starts at Bit 24 within assigned slot.		
		100	AGC_GAIN4 data starts at Bit 32 within assigned slot.		
		101	AGC_GAIN4 data starts at Bit 40 within assigned slot.		
		110	AGC_GAIN4 data starts at Bit 48 within assigned slot.		
		111	AGC_GAIN4 data starts at Bit 54 within assigned slot.		
[4:0]	AGC_GAIN4_SLOT		Slot Used for Limiter Linking AGC_GAIN4	0x0	R/W
		0	AGC_GAIN data placed in Slot 1.		
		1	AGC_GAIN data placed in Slot 2.		
		10	AGC_GAIN data placed in Slot 3.		
		11	AGC_GAIN data placed in Slot 4.		
		100	AGC_GAIN data placed in Slot 5.		
		101	AGC_GAIN data placed in Slot 6.		
		110	AGC_GAIN data placed in Slot 7.		
		111	AGC_GAIN data placed in Slot 8.		
		1000	AGC_GAIN data placed in Slot 9.		
		1001	AGC_GAIN data placed in Slot 10.		
		1010	AGC_GAIN data placed in Slot 11.		
		1011	AGC_GAIN data placed in Slot 12.		
		1100	AGC_GAIN data placed in Slot 13.		
		1101	AGC_GAIN data placed in Slot 14.		
		1110	AGC_GAIN data placed in Slot 15.		
		1111	AGC_GAIN data placed in Slot 16.		

SOFTWARE RESET REGISTER

Address: 0x2E, Reset: 0x00, Name: SOFT_RESET

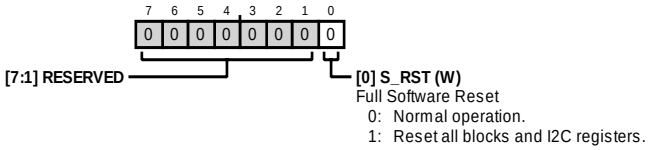

Table 56. Bit Descriptions for SOFT_RESET

Bits	Bit Name	Settings	Description	Reset	Access
[7:1]	RESERVED		Reserved.	0x0	R
0	S_RST		Full Software Reset	0x0	W
		0	Normal operation.		
		1	Reset all blocks and I^2C registers.		

OUTLINE DIMENSIONS

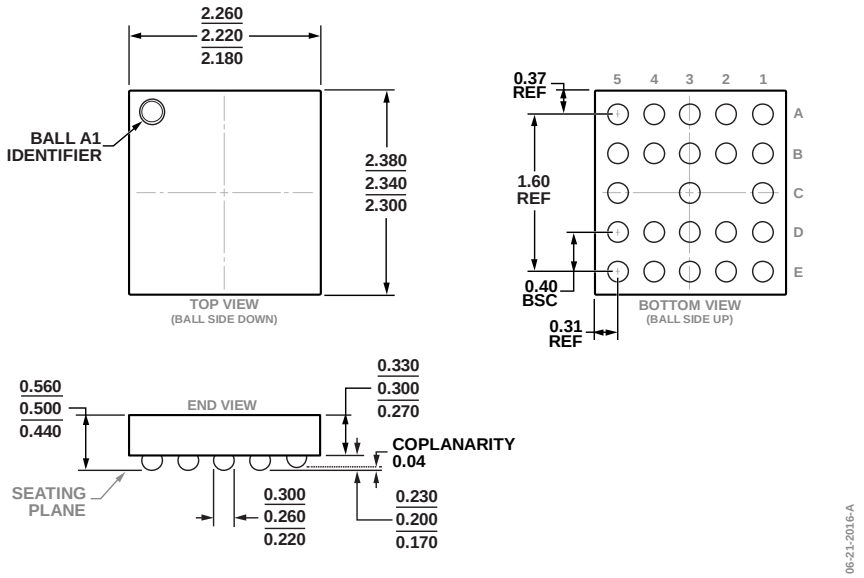

Figure 85. 23-Ball Wafer Level Chip Scale Package [WLCSP]
(CB-23-2)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
SSM3525BCBZRL	−40°C to +85°C	23-Ball Wafer Level Chip Scale Package [WLCSP]	CB-23-2
EVAL-SSM3525Z		SSM3525 Evaluation Board	

[1] Z = RoHs Compliant Part.

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