EMC2104

EMC2104
Silicon Errata and Data Sheet Clarification

TABLE 1: CHIP REVISION INFORMATION

Device ID = 1DH		
Functional Revision	**Revision Number**	**Part Marking (Note 1)**
B	01h	2104-1 Lot Number BCC
C	02h	2104-1 Lot Number CCC

Note 1: The Functional Revision Letter is the first letter of the third line of the part marking printed on the top of the package.

TABLE 2: DATA SHEET REVISION INFORMATION

	Part Number	**Specification Type**	**Revision Number**	**Date**
1.	EMC2104 (Rev B)	Data sheet	v1.59	08/21/2007
2.	EMC2104 (Rev C)	Data sheet	v1.60	08/27/2007

TABLE 3: ANOMALIES, SPECIFICATION CHANGES, AND ISSUES SUMMARY

Type	Functional Rev (Note 2)		Description
	B	**C**	
PWM1 Polarity Inverted	X	X	PWM1 Polarity Inverted
	X	X	PWM1 Polarity Bit
	X	-	TRIP_SET not Detecting Open State
	X	-	Look Up Table Enable
	X	-	Digital Pins Fail Latchup Test
	X	-	SYS_SHDN# Leakage Current
	X	-	Vdd Rise Time

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Type	Functional Rev (Note 2)		Description
	B	**C**	
Specification Changes	-	X	Default SpinUp Level
	-	X	Tcrit Registers Added
	-	X	New Hardware Failsafe Channel Option
	X	X	GPIO Drive Current
	-	X	GAINP and GAINI Weight
Issues	-	-	No Issues

2: 'X' = Indicates the Functional Rev which has the anomaly or in which a Specification Change was implemented; '–' = Not Applicable to the Functional Rev.

Silicon Errata Issues

Errata 1:   PWM1 Polarity Inverted

The PWM1 output is inverted so it is logic high when in the fan OFF condition.
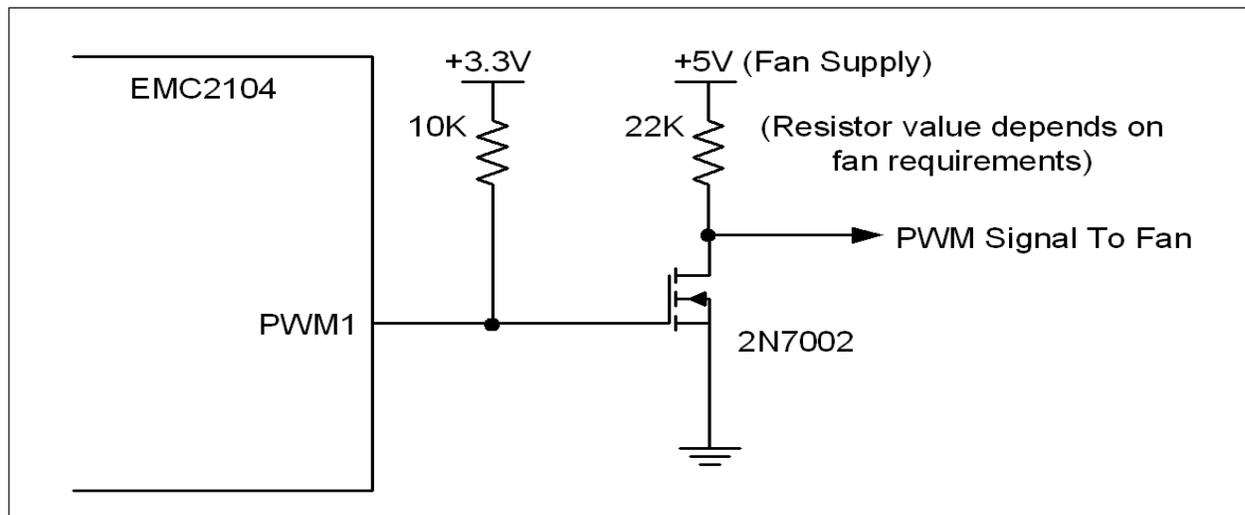
END USER IMPLICATIONS

This polarity inversion is opposite of the requirements for directly driving most 4-wire fans.

Work Around

A signal inversion must be added. A typical circuit is shown in Figure 1.

FIGURE 1:   PWM DRIVE SIGNAL INVERSION

Errata 2:   PWM1 Polarity Bit

DESCRIPTION

Register 0x2A, bit 0 does not control the PWM1 polarity as specified.

END USER IMPLICATIONS

The polarity of PWM1 cannot be changed.

Work Around

The external drive circuit must provide any polarity inversions required by the application.

Errata 3:   TRIP_SET not Detecting Open State

DESCRIPTION

The TRIP_SET pin is not detecting an "OPEN" condition.

END USER IMPLICATIONS

This anomaly will set the T_{TRIP} value to the maximum temperature available (122C or 154C) if a resistor is not in place. This "OPEN" condition is not a desired condition, but rather a fail safe for manufacturing defects in the resistor or assembly of the final product.

Work Around

If the minimum temperature for T_{TRIP} (60C or 92C) is desired, a short to ground is required. This anomaly will be corrected in Functional Revision C.

Errata 4: **Look Up Table Enable**

DESCRIPTION

When enabling LUT1 or LUT2, the corresponding fan output will enter spinup regardless of current fan setting.

END USER IMPLICATIONS

The fan will have a noticeable surge anytime the respective look up table is enabled.

Work Around

This anomaly will be corrected in Functional Revision C.

Errata 5: **Digital Pins Fail Latchup Test**

DESCRIPTION

The digital I/O pins fail Latchup Testing. The pins affected include pin 5 through pin 16: OVERT3#/GPIO5/PWM4, ALERT#, CLK_IN/GPIO1, OVERT2#/GPIO4/PWM3, SYS_SHDN#, SMDATA, SMCLK, GPIO6, PWM2/GPIO3, TACH2/GPIO2, TACH1, and OVERT1#/PWM1.

To cause latchup on these pins, the input signal needs to be pulled below ground and greater than 20mA must be drawn from the pin; the specification for this test requires the pin to withstand greater than 150mA.

END USER IMPLICATIONS

If this event occurs, power-cycling is required to restore normal operation. However, it is not expected that such a signal can be generated on actual application boards.

Work Around

This anomaly will be corrected in Functional Revision C.

Errata 6: **SYS_SHDN# Leakage Current**

DESCRIPTION

The leakage current when Vdd=0 is greater than specified. If SYS_SHDN# is pulled up to a voltage of 3-5Vdc when the supply pin Vdd = 0, the leakage current can be up to 30uA. The leakage current increases with voltage and temperature.

END USER IMPLICATIONS

This anomaly may result in an undesirable power consumption and voltage drop across the pullup resistor.

Work Around

This anomaly will be corrected in Functional Revision C. To minimize the leakage current, use the lowest pullup voltage possible.

Errata 7: **Vdd Rise Time**

DESCRIPTION

Some Vdd rise times (also called supply ramp rate) may result in improper internal initialization. The susceptible rise times vary from part to part and somewhat with temperature so it is not possible to specify a maximum rise time for correct operation.

END USER IMPLICATIONS

The EMC2104 will be inoperable if this anomaly occurs. It will not be damaged and cycling power may restore proper operation.

Work Around

This anomaly is corrected in Functional Revision C. As a workaround, decreasing the Vdd rise time generally results in normal operation.

Specification Changes

The Specification Changes described below are detailed in Data Sheet V1.60, dated 8-27-07.

DEFAULT SPINUP LEVEL

The default SpinUp Level is changed from 30% to 60% in Functional Revision C. Some fans, especially when driven by linear drive circuits cannot start at 30%. The higher default SpinUp Level will reduce the possibility of repeated SpinUp routine executions. The programmer can simply set the SpinUp Level to the required value with Functional Revision B; changing the default will reduce confusion due to the fan not starting properly.

TCRIT REGISTERS ADDED

To increase the flexibility of the software-programmed temperature channels that can trigger SYS_SHDN#, independent Tcrit Limit and Status registers will be added in Functional Revision C. These limits are "Write-Once and Lock" and cannot be changed once written. If these limits are exceeded, the SYS_SHDN# pin will be asserted. Operation is similar to setting the SYSx bits in configuration register 20h, but utilizes independent Tcrit Limit Registers for added flexibility, allowing the temperature channels' high and low limits to assert the ALERT# pin without triggering the SYS_SHDN# pin.

NEW HARDWARE FAILSAFE CHANNEL OPTION

To permit the Internal temperature channel to be used as the hardware-programmed channel, an additional option will be added in Functional Revision C. The SHDN_SEL pin's decode options will be modified so that the Internal channel can be used as the hardware-programmed channel.

The "Disabled" decode selection will be re-deployed as the Internal Temperature hardware-strapped option.

The behavior of the TRIP_SET input is different in this mode. While the TRIP_SET voltage setting can normally be created with a single resistor to ground, when the internal temperature channel is selected a resistor divider is required. Consult the data sheet for the formula which describes this resistor divider.

GPIO DRIVE CURRENT

The Voh specification of Vcc-0.4V is marginal at 8mA. The drive current value will be changed to 4mA.

GAINP AND GAINI WEIGHT

The weight of the Proportional and Integral Gains factors have been modified in Revision C. GAINP is increased by x2, while GAINI is decreased by X4. This change can increase the responsiveness when fast changes are needed. It does not affect applications where Ramp Rate Control is employed, i.e. the step size is limited.

Issues

NO ISSUES

APPENDIX A: DOCUMENT REVISION HISTORY

Revision Level	Description
REV A (03-11-14)	REV A replaces previous SMSC version v0.92 (10/31/07)
v0.92 (10/31/07)	Added Vdd Rise Time anomaly and GAINI and GAINP Weight Specification Change
v0.91 (09/25/07)	Clarified Data Sheet Revisions, cosmetic chgs
v0.9 (09/10/07)	Initial Release for Engineering Review

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